DIGITAL LABII MANUAL

EEC -452

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CONTENTS

SYLLABUS FOR DIGITAL LAB II

EEC -452: Digital Lab II

1. TTL transfer characteristics and TTL IC gates.
2. CMOS Gate Transfer Characteristics.
3. Implementation of a 3 bit SIPO and SISO shift registersusing flip-flops.
4. Implementation of a 3 bit PIPO and PISO shift registersusing flip-flops.
5. Design of seven segment display driver for BCD codes.
6. BCD Adders and Subtractors.
7. ALU
8. 8085 Assembly Language Programming.

STUDY AND EVALUATION SCHEME

SESSIONAL EVALUATION:-

CLASS TEST	**:**	**10 MARKS**
TEACHER'S ASSESMENT	**:**	**10 MARKS**
EXTERNAL EXAM	**:**	**30 MARKS**
TOTAL	**:**	**50 MARKS**

LIST OF EXPERIMENTS

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1. TTL transfer characteristics and TTL IC gates.
2. CMOS Gate Transfer Characteristics.
3. Implementation of a 3 bit SIPO and SISO shift registersusing flip-flops.
4. Implementation of a 3 bit PIPO and PISO shift registersusing flip-flops.
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INDEX

S.NO.	NAME OF EXPERIMENT	DATE OF EVALUATION	GRADE

EXPERIMENT - 1

Aim:To study the TTL transfer characteristics and TTL IC gates.

Apparatus Required

1. Trainer Board

2. Patch cords

3. Oscilloscope

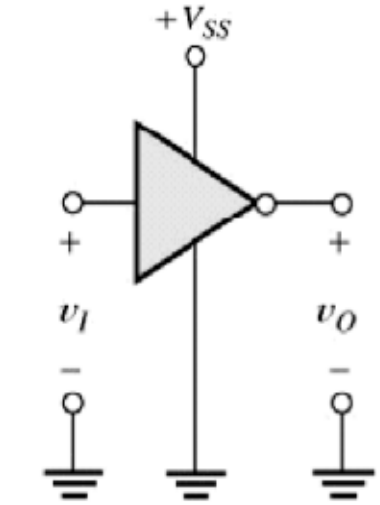
4. Two Digital Multimeters

Theory:-

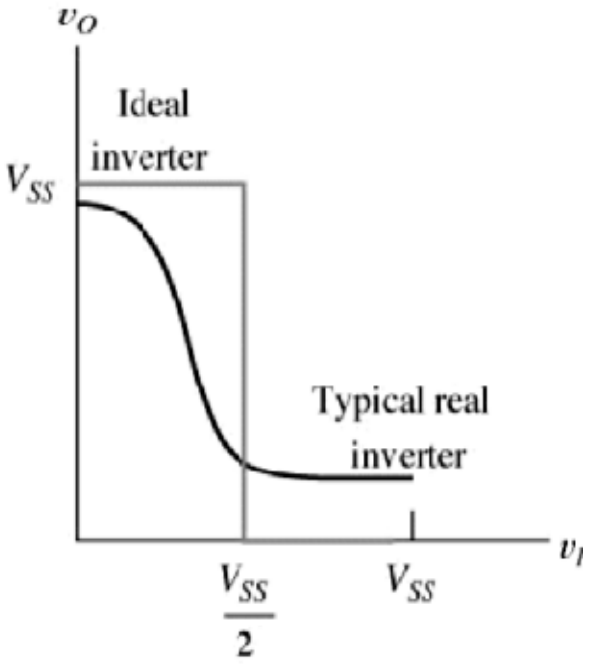
Voltage Transfer Characteristics :

The static voltage transfer characteristic of a logic gate is simply a plot of the gate outputvoltage V_{OUT} versus the gate input voltage V_{OUT}. We can mathematically describe thetransfer characteristic as $V_{OUT} = f(V_{IN})$. We use the word static to describe the transfercharacteristic because it represents behaviour in response to slowly changing signals so thatdynamic effects such as the delaying of the signal from gate input to gate output areavoided in measurements.Figure shows an ideal static transfer characteristic for an inverter with input V_{IN}, output V_{OUT} and power supply voltage VCC. The operating pointsof the inverter corresponds to the High and Low values on the outputs of theinverter. Since the output voltage depends on the input voltage, to find the value of thehigh operating point for an inverter output, the value of the low operating point for thesame inverter needs to be applied to its

input. Likewise, to find the value of the Lowoperating point, the value of the High operating point needs to be applied. By analytically using feedback, wecan combine the transfer characteristics of two identical inverters to achieve thisdependency relationship.



(a) Symbol including power-supply connections (often not shown)



(b) Transfer characteristics

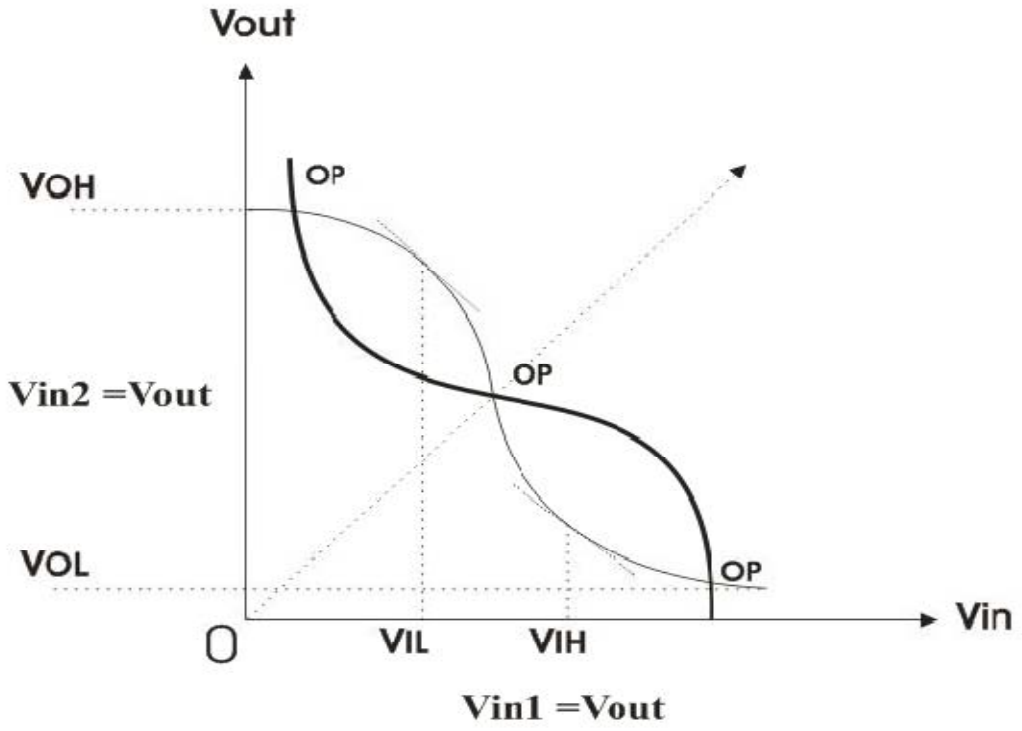


Figure 1(c) : Transfer Characteristic and Operating Points

This is done by connecting two inverters in a loop as shown in Figure 1(C). For the twoinverters, we note that VIN2 = VOUT1 and VIN1 = VOUT2. Since both of the invertershave the same transfer characteristic, we take the transfer characteristic of inverter 2 andmirror it about the VOUT = VIN line so that its VIN axis lies coincident with the VOUTaxis of the transfer characteristic for inverter 1 as shown in Fig. 1-1(b); then the VIN axisof gate 1 also coincides with the VOUT axis of gate 2. By this mirroring operation, therelationships given in Fig. 1-1(c) are satisfied on the axes of the plot. Because of thevoltage equalities, the only points where both static transfer characteristics can besatisfied on this plot are where they intersect. These intersection points are (VIN1 = 0.15V, VOUT1= 4.05 V), (VIN1 = 1.50 V, VOUT1 = 1.50 V), and (VIN1 = 4.05 V, VOUT1 =0.15 V); these operating points are marked with OP.A small change in VIN1 from 1.5 V will cause departure from the (VIN1 = 1.5V, VOUT1 = 1.5 V) point toward one of the other two points. Thus, this point is unstable,will not persist, and is of little interest.

Small departures from the other two operatingpoints, however, are reversible and with the appropriate change in VIN1 will result in areturn to those points. These are stable operating points for the inverters. They define thevoltage values that correspond to High and Low on inputs and outputs of this particularinverter. Since we are using positive logic, High corresponds to 1 and Low corresponds to0. Thus for the given inverter, the voltage values for 0 and 1 are 0.15 V and 4.05 Vrespectively. For VOUT, the Low value is V output Low, denoted VOL, and the High value, Voutput high, denoted VOH. So, for this inverter, VOL is 0.15 V and VOH is 4.05 V. Finally, sincethe Low value on the input produces a High value on the output and vice-versa, an inversion ofthe voltage values has occurred. For either positive or negative logic, the inverter is also oftencalled a Not gate since it negates the input value to produce the output value.

Procedure:

Voltage Transfer Characteristics :

1. Make the connection as shown in the figure .
2. Now increase the input voltage in small steps using knob Vin and note down thecorresponding values of the output voltage.
3. To get a fine shape of the transfer curve at the knees take sufficient point for yourobservation near the transition region and then draw the graph between input andoutput voltages.
4. This is the required voltage transfer characteristics for a TTL inverter.

VTC Observation On Oscilloscope :

We can also directly view the complete transfer curve on your CRO screen. Follow the

following steps:

1. Switch off the power supply to the board. Then connect the input of the inverter to triangularwave output of Function generator.

2. Take care of the fact that the maximum amplitude of the triangular input should not exceed themaximum limits of the device under test. For TTL inverter the maximum amplitude of thetriangular input should be kept between 4-5 Volts.

3. Connect this same input to the X-channel of the CRO and connect the other CRO input i.e. Ychannelto the output of the inverter and press XY mode switch of CRO.

4. You will observe the complete transfer characteristics on the CRO screen. If however the view isnot symmetrical or not in expected shape then just adjust the settings of CRO to get the clearpicture. Also you can change the input triangular wave amplitude within tolerable limits to get the perfect view of the VTC.

Result:-

The voltage transfer characteristics are observed. Observed output matches theoretical concepts.

Precautions:-

- All connections should be made neat and tight.
- Digital lab kits should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.

Pre Questions:-

1) What is the voltage transfer characteristic of a logic gate?
2) What is the average time delay in basic gate?
3) What is the packing density of TTL gate?

Post Questions:-

1) TTL operates from a _____volt supply.
2) What is thevoltage range of logic 0 and logic 1?
3) In what aspect TTL is better than CMOS

EXPERIMENT – 2

Aim: - Study of CMOS Gate Transfer Characteristics.

Apparatus required: -

1. Trainer Board
2. Patch cords
3. Digital Oscilloscope.
4. Two Digital Multimeters

Theory:

CMOS logic is exemplified by its extremely low power consumption and high noise immunity.Hence, it is prevalently used in devices demanding low power dissipation, such as digitalwristwatches and other battery powered devices, or in devices operated in noisy environments,such as industrial plants. A wide variety of CMOS logic devices in the 4000 series are available.Unlike TTL logic, CMOS logic requires two supply voltages, VDD and VSS. In typical logicaldesigns, VDD ranges from +3 V to +16 V. The other supply, VSS, is normally grounded.Also, the physical representation of the binary states in CMOS logic is not entirely compatiblewith TTL logic. As a consequence of CMOS's extremely high input impedance, the logic levelsin CMOS systems are essentially VDD and ground. If, for example, a 5 volt power supply isused, LOW typically ranges from 0 to 0.01 V and HIGH from 4.99 to 5.0 V for CMOS outputs.

Input voltages ranging from 3.5 to 5 V are recognized as HIGH and voltages from 0 to 1.5 V asLOW.It may appear that CMOS output logic levels, using a 5 V power supply, completely conform tothe TTL logic level ranges of 0 to 0.8 V for LOW and 2.0 to 5.5 V for HIGH. However, thevoltage level ranges representing HIGH and LOW are not the only factors that determinewhether two logic family are compatible or not. The amount of current that can be supplied byoutputs and that can be assimilated by inputs of gates within each logic family is

anotherconsideration. Specifically, when CMOS drives TTL logic, the crucial question is whether theCMOS output, in the LOW state, can sink enough of the current originating at the TTL input toensure that the voltage at the TTL input does not exceed its maximum LOW level input voltageof 0.8 V. Typical CMOS gates can sink about 0.4 mA in the LOW state while maintaining anoutput voltage of 0.4 V or less. This is sufficient to drive two low-power TTL inputs, butgenerally insufficient to drive even one standard TTL input. In any case, loss of dc noiseimmunity is an inevitable result. It is better to use a special buffer such as a 74C901 to drivestandard TTL from CMOS. The HIGH state poses no problems.Similarly, improper circuit operation may result from connecting TTL outputs to CMOS inputs.In the LOW state, a TTL output can drive CMOS directly. However, the guaranteed TTL HIGHoutput level of 2.4 volts is not a valid input level for CMOS. If the TTL output drives onlyCMOS inputs, then essentially no current is drawn and the HIGH output may be 3.5 V or higher.Whether this is sufficient for reliable operation depends upon the exact specifications forboth the TTL outputs and the CMOS inputs.

CMOS CHARACTERISTICS

The **voltage transfer curve** for a typical CMOS logic gate is shown in Figure . Note that thecurves in the transition region are almost vertical. This narrow transition region is the reason forCMOS logic's high noise immunity. Not much voltage range is covered in the transition fromone state to the other. In contrast to TTL devices, the threshold voltage depends on the supplyvoltage and is approximately half the supply voltage.As with TTL logic, **current spiking** occurs during switching. Hence, bypass capacitors are usedin CMOS logic design as well.

However, they are not as critical as in TTL logic design becauseof CMOS's high noise immunity.Whereas the typical **quiescent (static) power dissipation** (power dissipation of a device that isnot changing logic states) of TTL IC's was about 40 mW, the power dissipation of CMOS IC'sare typically 25 nW. However, as the frequency of switching increases, **dynamic powerdissipation** becomes important, as illustrated in Figure. Above 1 MHz, the dynamic powerdissipation predominates and can exceed TTL power dissipation.

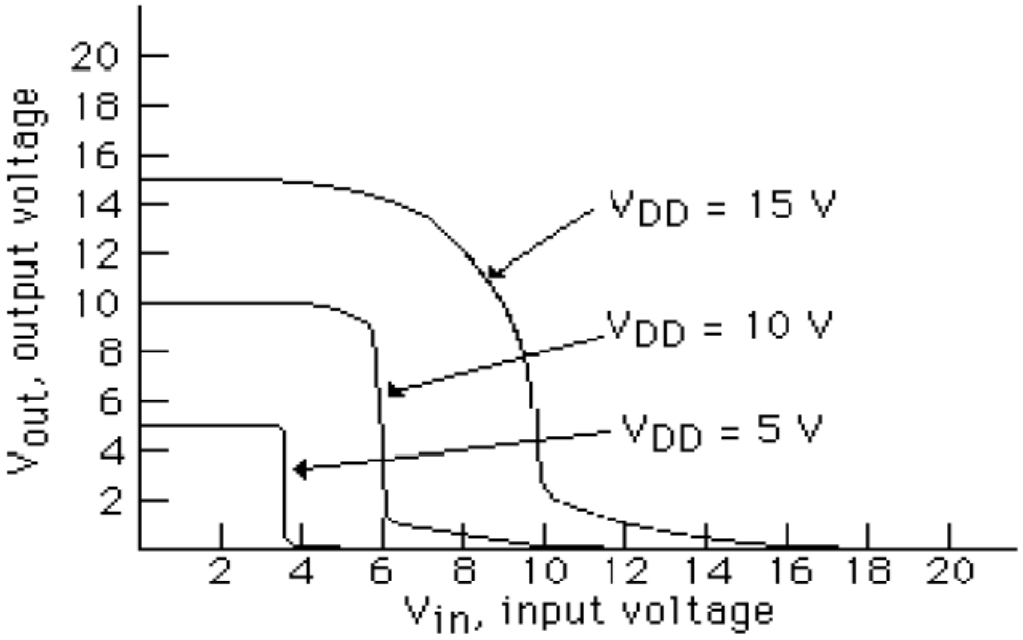


Fig: CMOS Voltage Characteristics

Procedure:

1. Switch on the power supply of NV6551A board
2. Out of the two supply connect 12V to Vdd for CMOS devices.

● **Voltage Transfer Characteristics :**

3. Make the connection as shown in the figure above.
4. Now increase the input voltage in small steps using knob Vin and note down thecorresponding values of the output voltage.

5. To get a fine shape of the transfer curve at the knees take sufficient point for yourobservation near the transition region and then draw the graph between input and outputvoltages.

6. This is the required voltage transfer characteristics for a CMOS inverter.

● **VTC Observation On Oscilloscope :**

You can also directly view the complete transfer curve on your CRO screen. Follow thefollowing steps:

7. Switch off the power supply to the board. Then connect the input of the inverter totriangular wave output of Function generator.

8. Take care of the fact that the maximum amplitude of the triangular input should notexceed the maximum limits of the device under test. For CMOS inverter the amplitude ofthe triangular input should be kept between 4-5 Volts.

9. Connect this same input to the X-channel of the CRO and connect the other CRO inputi.e. Y-channel to the output of the inverter and press XY mode switch of CRO.

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Result: The voltage transfer characteristics are observed. Observed output matches theoretical concepts

Precautions:-

- All connections should be made neat and tight.
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- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.

Pre Questions

1) What is the static power consumption in CMOS?
2) How many different regions are there on CMOS transfer characteristics?
3) Which region is unstable on CMOS transfer characteristics?

Post Questions

1) Ideally what should be the output voltage for logic 0?
2) What should be the output voltage for logic 0 in order to have maximum possible noise margin?
3) What should be the width of transition region in order to have a larger noise margin?

EXPERIMENT - 3

Aim:- Implementation of a 3 bit SIPO and SISO shift registers using flip-flops.

Apparatus: -

1.trainer board

2. 2 mm patch chords

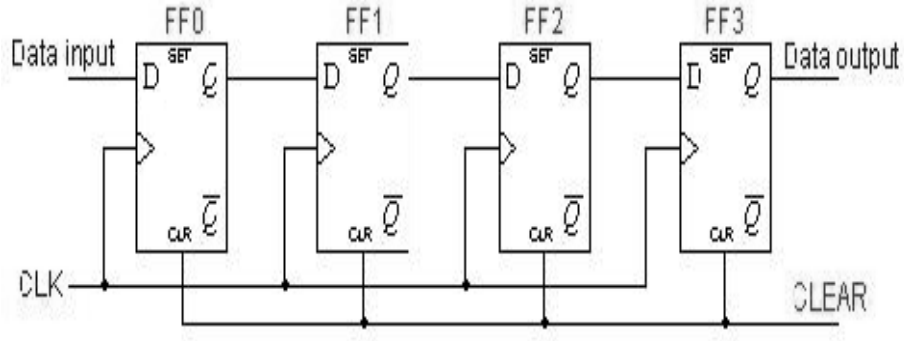
3. +5V adaptor

Theory: -

A register is a group of binary storage cells suitable for holding binary information. Agroup of flip-flops constitute a register. Since each flip-flop is a binary cell capable ofstoring one bit of information, a n-bit register has a group of n flip-flops and is capable ofstoring any binary information containing n bits. In addition to the flip-flops, a registermay have combinational gates that perform certain data processing tasks like when andhow new information is transferred in to the register.
A register capable of shifting its binary information either to the right or to the left iscalled a shift register. The logical configuration of a shift register consists of a chain offlip-flops connected in cascade, with the output of one flip-flop connected to the input ofnext flip-flop. Here, all the flip-flops receive a common clock pulse, which causes thedata bits to shift from one stage to the next.Shift
registers may be configured so that the stored data may be moved in more than one direction. They may be configured so that data may be entered and stored from multipleinputs. They may be grouped into arrays of two or more dimensions in order to performmore complex data operations.

One method of describing the shift register characteristics is, by how data is loaded intoand is read from the storage units. Depending on this characteristic, shift registers areclassified into four types:
1. Serial in-serial out shift register
2. Serial in-parallel out shift register
3. Parallel in-serial out shift register
4. Parallel in-parallel out
The fundamental ideas behind the operation of the four types of shift registers illustratedin below with the help of diagrams:

1. Serial in serial out shift register:



A basic 4-bit shift register can be constructed using four D flip-flops, as shown in abovefigure. The register is first cleared, forcing all four outputs to zero. The input data is thenapplied sequentially to the D input of the first flip-flop from the left (FF0). During eachclock pulse, one bit is transmitted from left to right. The least significant bit (LSB) of thedata is the first to be shifted through the registers i.e. from FF0 to FF3.

In order to get the data out of the register, they must be shifted out serially. This can bedone destructively or non-destructively. In a destructive readout, the original data is lostand at the end of the read cycle, all flip-flops are reset to zero. To avoid the loss of data,an arrangement for non-destructive reading can be done by adding two AND gates, anOR gate and an inverter to the system. The construction of this circuit is shown below.The data is loaded to the register when the control line is high.

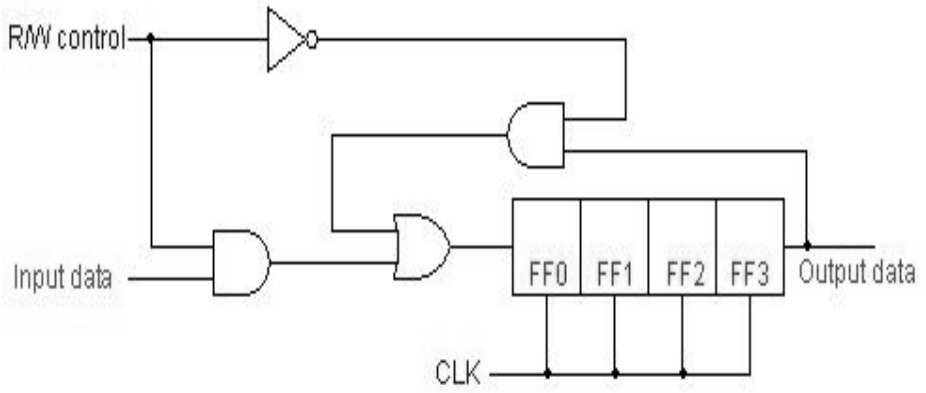


Figure 2

The data is loaded to the register when the control line is HIGH (i.e. WRITE). The data can be shifted out of the register when the control line is LOW (i.e. READ).

2. Serial in parallel out shift register:

In this kind of register, data bits are entered serially in the same manner as discussedabove. The difference is the way in which the data bits are taken out of the register. Oncethe data are stored, each bit appears on its respective output line, and all bits are availablesimultaneously. A construction of a 4-bit serial in parallel out register is shown below.

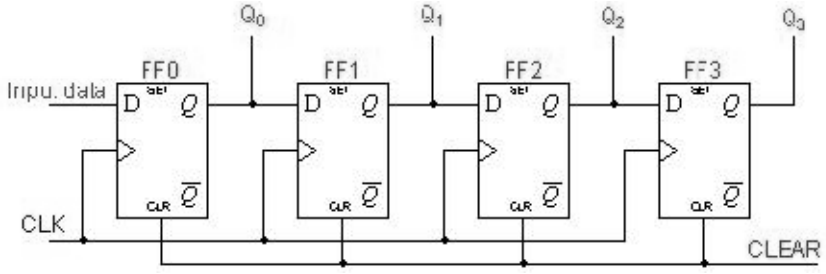


Figure 3

The Q output of a given flip-flop is connected to the D input of the next flip-flop to itsright. The serial input determines what goes into the leftmost flip-flop during the shift.Each positive edge of the clock pulse transition shifts the contents of the register one bitposition to the right. The serial output is taken from the output of

rightmost flip-flop priorto the application of clock pulse. There are four parallel outputs Q0-Q3 with Q3 as LSB.The CLEAR input is an active low input to the flip-flops. It resets or clears the outputsQ0-Q3 when low.

Truth Table:
(Logic 1= +5 V & Logic 0= GND; 0 → 1 = Positive Edge trigger)

CLOCK PULSE NO.	PRESET	CLR	CLK	D0	Q3
0	1	0	1	1	0
1	1	1	0→ 1	1	0
2	1	1	0→ 1	0	0
3	1	1	0→ 1	1	0
4	1	1	0→ 1	0	1
5	1	1	0→ 1	0	0
6	1	1	0→ 1	0	1
7	1	1	0→ 1	0	0
8	1	1	0→ 1	0	0

Table: Truth table for 4-bit serial in serial out shift register

Procedure:

1. Connect +5 V adaptor to its indicated position on the trainer board for power supplybut do not switch it 'ON'.

2. Connect serial data input D0 to I0 of output section. Toggle it to logic 1 level.

3. Connect the CLK socket using patch cords to socket A of CLK IN. Toggle it to logic 1 level .Clear the outputs Q0-Q2 by toggling CLK IN to logic 1 level.

4. Connect PRESET input to I1 of input section. Toggle it to logic 1 level.

5. Connect CLR input to I2 of input section respectively. Toggle it to logic 0 level

6. Connect the serial data output Q2 to O0 of output section.

7. Now switch 'ON' the power supply.

8. Observe output on LED display of O0 in the output section**.** It will be off or at logic0 level.

9. Now connect logic 1 to CLR input.

10. Give logic 0 to 1 transition at the CLK IN switch.

11. Observe output on LED display of O0 in the output section**.** It will be still off or atlogic 0 level.

12. Repeat steps 10-11 and you will observe that the output displays logic 1 or led glows after 3 positive or 0 to 1 clock transitions.

13. Toggle I0 connected to D0 for different inputs from clock pulse number 2-7 as pertruth table 2 and verify the truth table.

14. You can also check outputs of all the flip-flops simultaneously for more detailed illustration of the shift operation. You just have to connect the outputs Q0-Q2 of flip-flops to the sockets O0-O2 in output section.

RESULT:

Precaution:-

- The circuit should be off before change the connections.
- Digital lab kits should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- .After completing the experiment switch off the supply to apparatus.

Pre Questions:-

1) How much storage capacity does each stage in a shift register represent?

2) How many clock pulses must be there to serially shift a nibble (four bits) of data into a shift register?

Post Questions:-

1) **How many clock cycles are needed in order to have first output in SISO?**
2) **How many clock cycles are needed in order to have all the outputs after feeding the inputs?**
3) **What is the application if SISO and SIPO?**

EXPERIMENT -4

Aim: - Implementation of a 3 bit PIPO and PISO shift registers using flip-flops

Apparatus:

1. NV6561 trainer board

2. 2 mm patch chords

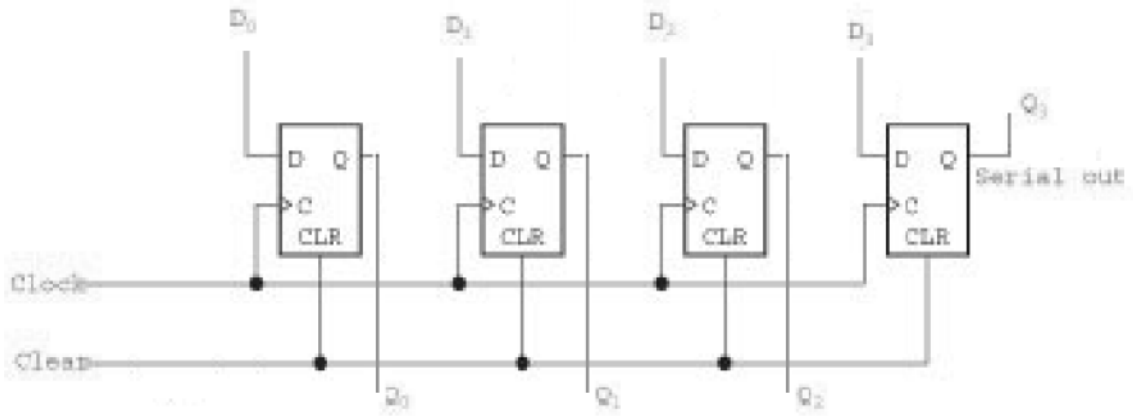
3. +5 V adaptor

Theory:

Parallel in serial out shift register:

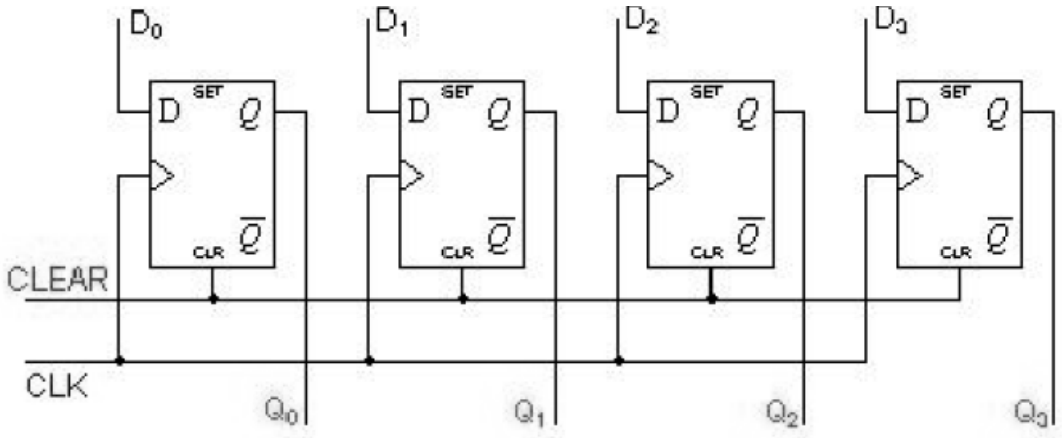
A 4-bit parallel in serial out shift register is shown below. The circuit uses D flip-flopsand NOR and AND gates for entering or loading data (i.e. writing) to the

register.D0, D1, D2 and D3 are the parallel inputs, where D0 is the most significant bit and D3 isthe least significant bit. To load or write data, the mode control line is taken LOW andthe data is clocked in. The data can be shifted when the mode control line is HIGH asSHIFT is active high. The register performs right shift operation on the application of aclock pulse.



Parallel in parallel out shift register:

The following circuit is a four-bit parallel in parallel out shift register constructed by D flip-flops. In case of parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits.



In the above figure, the D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously**.** And with help various control lines can be shifted to either right or left direction i.e. either from FF0 to FF3 or vice versa.

Truth Table:
(Logic 1= +5 V & Logic 0= GND; 0 → 1 = positive edge trigger)

CLOCK PULSE NO.	SHIFT/ LOAD'	CLK INH	CLK	D1	D2	D3	Q3
0	0	*x*	*x*	0	0	0	0
1	0	0	0→ 1	0	1	1	1
2	1	0	0→ 1	0	1	1	1
3	1	0	0→ 1	0	1	1	0
4	1	0	0→ 1	0	1	1	1
5	1	0	0→ 1	0	1	1	1
6	1	0	0→ 1	0	1	1	0

Table : Truth table for 3-bit parallel in serial out shift register

Procedure:

1. Connect +5 V adaptor to its indicated position on the trainer board for power supply but do not switch it 'ON'.

2. Connect the inputs D1-D3 of 3-bit parallel in serial out shift register section to I2-I4 of input section.

3. Connect serial data output Q3 to O0 of output section. Toggle it to any position as you want.

4. Connect the CLK socket using patch cords to socket A of CLK IN. Toggle it to any position as you want.

• For parallel loading of data at input

5. Connect the CLK INH input to I1 of input section. Toggle it to any position as you want.

6. Connect the SHIFT/LOAD' input to I0 of input section. Toggle it to logic 1level.

7. Switch 'ON' the power supply.

8. Now load whatever input you want (e.g. 011 as per the truth table 6) at the four inputs. For this, you have to toggle the switches corresponding to theinputs D1–D3 at the respective logic levels.

• **For serial shift of inputs**

9. Toggle the switch corresponding to CLK INH input i.e. I1 to logic 0 level.

10. Toggle the switch corresponding to SHIFT/LOAD' input i.e. I0 to logic1level.

11. Connect the CLK socket using patch cords to socket A of CLK IN. Give logic 0 to 1 transitions to CLK input.

12. Observe outputs on LED display of the output section**.** It will be reverse ofwhat you had loaded earlier. The LSB or input at D3 will be shifted anddisplayed first (i.e. if your input was 011, the output will first display 1, then 1and then 0).

13. Verify the truth table.

RESULT:-Truth table is verified

Precautions:

- Digital lab kits should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.

Pre Questions:

1) How many D flip- flops are needed for the implementation of 6 bits PIPO?
2) Which type of flipflops can be used for shift register?

Post questions

1) In a parallel in/parallel out shift register, $D_0 = 1$, $D_1 = 1$, $D_2 = 1$, and $D_3 = 0$. After three clock pulses, what is the data outputs?

EXPERIMENT-5

Aim:- Design of seven segment display driver for BCD codes

Apparatus: -

IC7447, 7-Segment display (common anode), Patch chords, resistor (1K) & IC Trainer Kit

THEORY:

The Light Emitting Diode (LED) finds its place in many applications in these modernelectronic fields. One of them is the Seven Segment Display. Seven-segment displayscontains the arrangement of the LEDs in “Eight” (8) passion, and a Dot (.) with a commonelectrode, lead (Anode or Cathode). The purpose of arranging it in that passion is that we canmake any number out of that by switching ON and OFF the particular LED's. Here is theblock diagram of the Seven Segment LED arrangement.

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anode legs uses only one cathode, which is common.Common Anode (CA)-The common leg for all the cathode is of Anode type.A decoder is a combinational circuit that connects the binary information from ‘n’ input linesto a maximum of 2^nunique output lines. The IC7447 is a BCD to 7-segment patternconverter.The IC7447 takes the Binary Coded Decimal (BCD) as the input and outputs therelevant 7 segment code.

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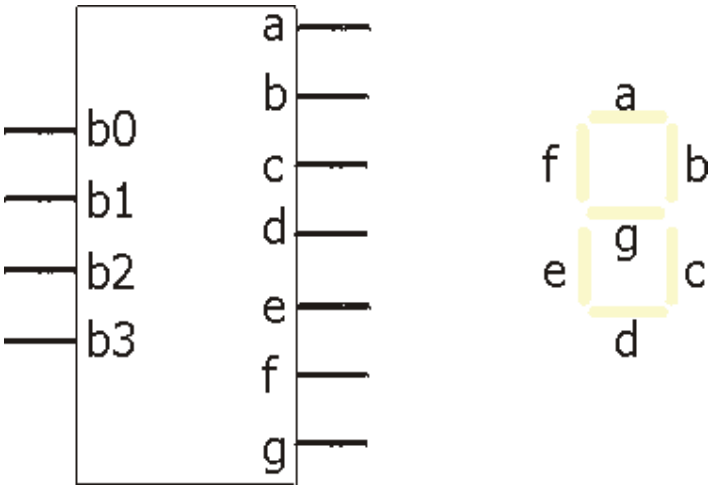


Figure 2. Control Logic map

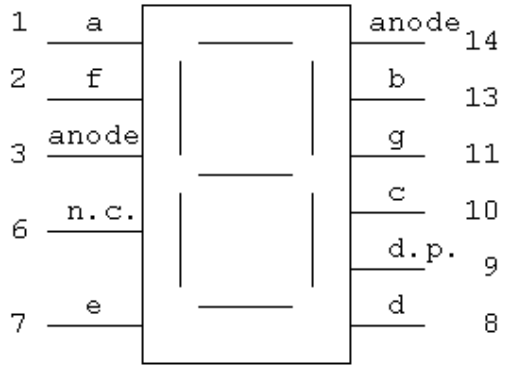


Figure 3. DSP-1 Pin out

Truth Table for BCD to 7 segment decoder

b3 b2 b1 b0	a b c d e f g
0 0 0 0	0 0 0 0 0 0 1
0 0 0 1	1 0 0 1 1 1 1
0 0 1 0	0 0 1 0 0 1 0
0 0 1 1	0 0 0 0 1 1 0
0 1 0 0	1 0 0 1 1 0 0
0 1 0 1	0 1 0 0 1 0 0
0 1 1 0	0 1 0 0 0 0 0
0 1 1 1	0 0 0 1 1 1 1
1 0 0 0	0 0 0 0 0 0 0
1 0 0 1	0 0 0 0 1 0 0
1 0 1 0	0110000
1 0 1 1	0110000
1 1 0 0	0110000
1 1 0 1	0110000
1 1 1 0	0110000
1 1 1 1	0110000

Figure 4. BCD -7 Segment Display Truth Table

PROCEDURE

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make the connections as shown in the circuit diagram.
4. Verify the truth table and verify the outputs.

Result: -The truth table and output is verified.

Precautions:-

1. All ICs should be checked before starting the experiment.
2. All the connection should be tight.
3. Always connect ground first and then connect Vcc.
4. Suitable type wire should be used for different types of circuit..
5. After completed the experiments switch off the supply of the apparatus

Pre Questions:-

1. What are the different types of LEDs?
2. Draw the internal circuit diagram of an LED.
3. What are the applications of LED.

EXPERIMENT-6

Aim: -Study of BCD Adders and Subtractors.

Apparatus:

NV6562 trainer board

2. +5 VDC adaptor

3. 2 mm Patch Cords

Theory:

The Adder / Subtractor:

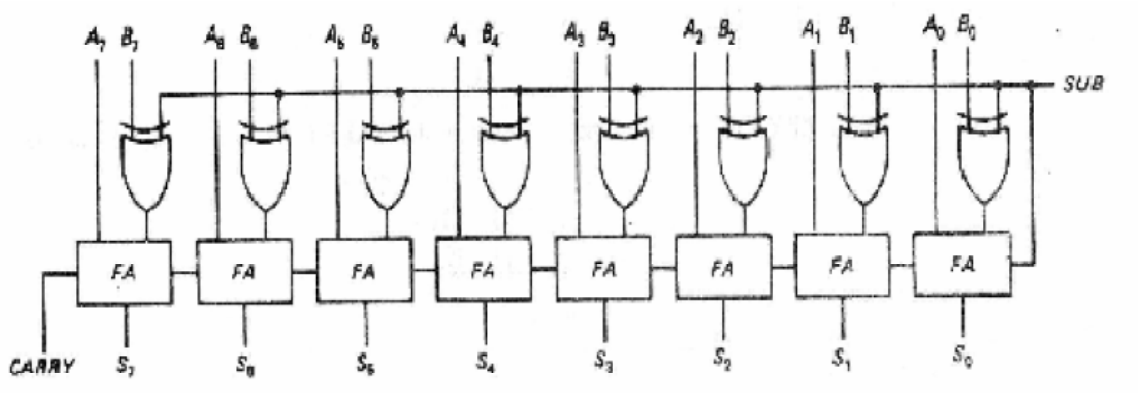
We can connect full adders as shown in the figure given below to add or subtract binary numbers. The circuit is laid out from right to left, similar to the way we add binary numbers. Therefore the least significant column is on the right, and the most significant column is on the left. The boxes labeled FA are full adders. The Carry out from each full adder is the carry in to the next higher full adder. The numbers being processed are A7 A6 A5 A4 A3 A2 A1 A0 and B7 B6 B5 B4 B3 B2 B1 B0, while the answer is S7 S6 S5 S4 S3 S2 S1 S0. With 8-bit arithmetic, the final carry is ignored for reasons given earlier. With 16-bit arithmetic, the final carry is the carry into the addition of the upper bytes.

Addition:

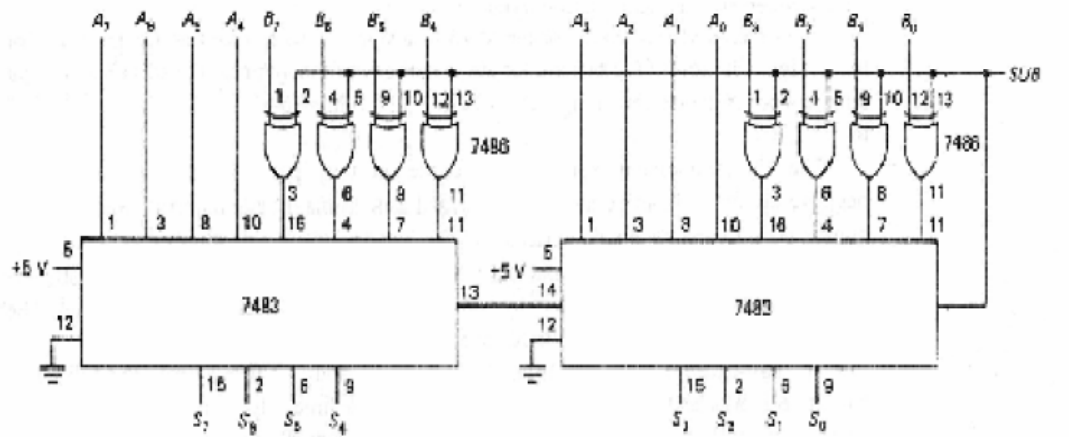
During an addition, the SUB signal is deliberately kept in the low state. Therefore thebinary number B7 B6 B5 B4 B3 B2 B1 B0 passes through the controlled inverter with nochange. The full adder then produces the correct sum.

Subtraction:

During a subtraction, the SUB signal is deliberately kept low. Therefore the controlledinverter produces the 1's complement of B7 B6 B5 B4 B3 B2 B1 B0. Furthermore, becauseSUB is the carry in to the first full adder, which is equivalent to adding 1 to t the 1'scomplement of B7 B6 B5B4 B3 B2 B1 B0 , and thus producing the correct result.



Figu



Procedure:-

1. Connect +5 V adaptor at the indicated position but do not switch on the PowerSupply initially.

2. Connect A0 and A1, B0 and B1 of IC7483 and IC 7486 to A0, A1 and B0,B1 of the input section respectively.

3. Also connect S0 and S1 of IC 7483 to the S0 and S1 of the output section.Then connect Add/Sub pin of input section to add/Sub pin of IC7483(4-Bitadder).

4. For 2-bit operation connect S2 of IC7483 to S2 of output section, this willact as output for carry (or borrow) generation.

5. For addition keep the ADD /SUB pin to zero level (if both the operands are positive numbers) so that all Bs bits pass unchangedthrough the controlled inverters and thus providing the correct sumoutput.

6. Now switch on the Power Supply.

7. For subtraction of Bs from As, keep ADD/SUB pin at logic 1 level. By thiswe are negating the Bs bits and then again adding it to As to get the desiredresult. Which is equal to A-B=S.

8. Pick the following example to verify your results:

(A1 – A0) + (B1 – B0) = (S1- S0)

11(As) + 11(Bs) = 110(SS) (3+3 = 6)

01(As) + 10(Bs) = 011(SS) (1+2 = 3)

11(As) - 01(Bs) = 010(SS) (3-1 = 2)

01(As) - 11 (Bs) = 110(SS) (1-3 = -2)

(A1 ……. A0) Where A1 is MSB and A0 is LSB.

(B1……. .B0) Where B1 is MSB and B0 is LSB.

(S1 …….. S0) Where S1 is MSB and S0 is LSB.

9. In case of generation of carry (or borrow) the LED at S2 will glow.

10. Observe the result at the output section; you can verify the result byperforming the operation manually.

Result:- The results are verified

Precautions:

- All connections should be made neat and tight.
- Digital lab kits should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- After completed the experiments switch off the supply of the apparatus.

EXPERIMENT-7

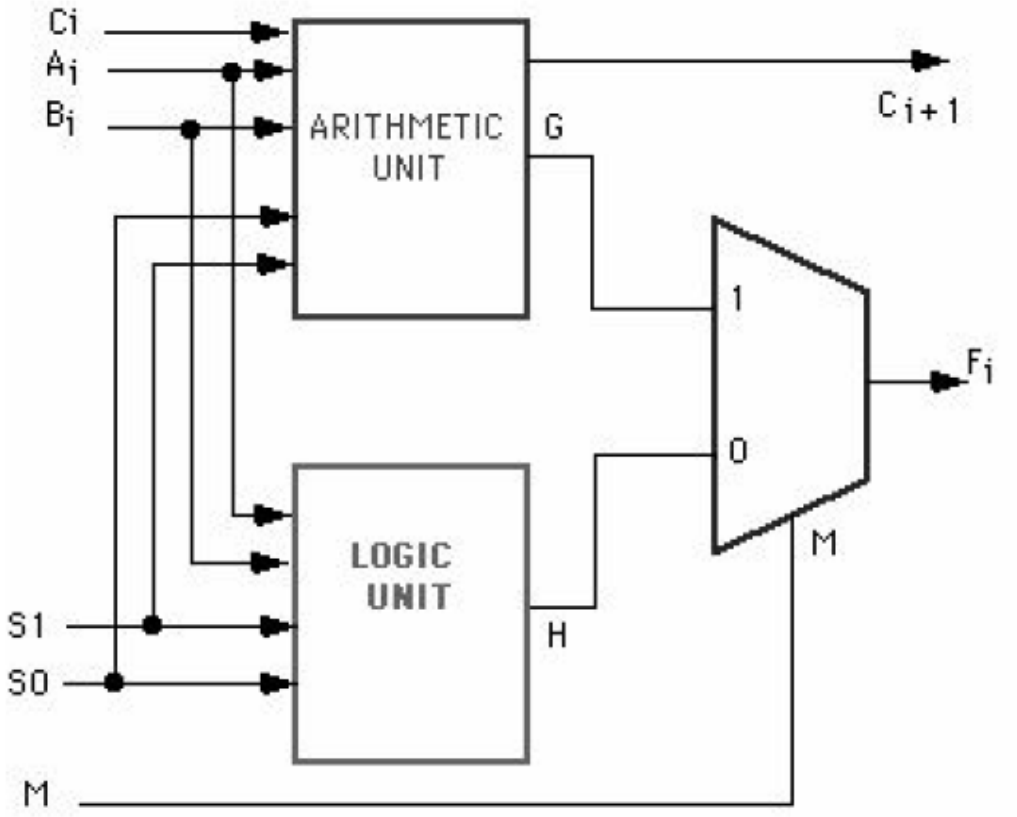
Aim:- To study ALU for performing logic' operation

Apparatus:

1. **NV6563** trainer board
2. Patch chords
3. +5V adaptor

Theory:-

The basic blocks of a computer are central processing unit (CPU), memory unit, andinput/output unit. CPU of the computer is basically the same as the brain of a humanbeing. It contains all the registers, control unit and the arithmetic logic unit (ALU).The ALU is the most important and fundamental building block of the central processingunit (CPU) of a computer, and even the simplest microprocessors contain one forpurposes such as maintaining timers. The processors found inside modern CPUs andgraphics processing units (GPUs) accommodate very powerful and very complex ALUsin which a single component may contain a number of ALUs.



In computing, an arithmetic logic unit (ALU) is a digital circuit that performs arithmeticand logical operations. It is a multi-operational, combinational-logic function thatperforms 2n logic and arithmetic micro-operations each, on a pair of n-bit operands. Thespecific operation that is performed by an ALU is determined by a specific binary codeapplied to its function-select inputs. These combinations of binary codes are interpreted within the ALU and the final output of the operation is obtained at output of ALU.Amore simpler diagrammatic representation of ALU is given below. Here,

A and B are the inputs (or operands) to the ALU

R is the output or result

F is the code or instruction (or op-code) from the Control Unit

D is output status; it indicates cases such as carry-in, carry-out, overflow, division-byzero.

Truth Table:

(Logic 1= +5 V & Logic 0= GND; M=1)

Step No.	Mode select lines M	Function Select Lines				Logic Functions F_n at $C_n = x$
		S3	S2	S1	S0	
1	1	0	0	0	0	$\overline{A}$
2	1	0	0	0	1	$\overline{A+B}$
3	1	0	0	1	0	$\overline{A} \cdot B$
4	1	0	0	1	1	Logical 0
5	1	0	1	0	0	$\overline{A \cdot B}$
6	1	0	1	0	1	$\overline{B}$
7	1	0	1	1	0	$A \oplus B$
8	1	0	1	1	1	$A \cdot \overline{B}$
9	1	1	0	0	0	$\overline{A}+B$
10	1	1	0	0	1	$\overline{A \oplus B}$
11	1	1	0	1	0	B
12	1	1	0	1	1	$A \cdot B$
13	1	1	1	0	0	Logical 1
14	1	1	1	0	1	$A + \overline{B}$
15	1	1	1	1	0	$A + B$
16	1	1	1	1	1	A

Note:

1. '*x*' means don't care.
2. '+' means Logical 'OR' function.
3. '•' means Logical 'AND' function.
4. '$\oplus$' means Logical 'XOR' function.
5. ' $\overline{\ }$ ' means Logical 'NOT' function.

Procedure:-

1. Connect sockets ‘ 0 - 3’ of ‘Input Section’ to sockets ‘ 0 - 3’ of ‘Arithmetic and Logic Unit’ section respectively.

2. Connect socket ‘Cn’ of ‘Input Section’ to socket ‘Cn’ of ‘Arithmetic and LogicUnit’ section.

3. Connect sockets ‘ 0 - 3’ of ‘Input Section’ to sockets ‘ 0 - 3’ of ‘Arithmetic andLogic Unit’ section respectively.

4. Connect sockets ‘S0–S3’ of ‘Function and Mode Select Input’ section to sockets‘S0-S3’ of ‘Arithmetic and Logic Unit’ section respectively.

5. Connect socket ‘M’ of ‘Function and Mode Select Input’ section to socket ‘M’ of‘Arithmetic and Logic Unit’ section.

6. Connect sockets ‘ 0- 3’ of ‘Output Section’ to sockets ‘ 0- 3’ of ‘Arithmetic andLogic Unit’ section respectively.

7. Connect sockets ‘Cn+4’, ‘A=B’, ‘ ’ and ‘ ’ of ‘Output Section’ to sockets ‘Cn+4’,‘A=B’, ‘ ’ and ‘ ’ of ‘Arithmetic and Logic Unit’ section.

8.Now give any combination of inputs at sockets ‘ 0 - 3’ and ‘ 0 - 3’ of Inputsection.

9. Toggle the mode control input ‘M’ to logic ‘1’ level for logic operation mode.

10. Now give any input to ‘Cn’ as you want.

11. Now toggle all the function select inputs ‘S0-S3’ to logic ‘0’ level.

12. Switch on the supply.

13. You will observe that the output is logical 1’s complement of input at ‘ 0 - 3’.Hence our output is logical ‘NOT’ function of ‘ 0 - 3’

Result: -Results are verified.

Precautions:-

1. All the connection should be tight.
2. Suitable type wire should be used for different types of circuit.
3. The kit should be off before change the connections.
4. After completed the experiments switch off the supply of the apparatus.

EXPERIMENT-8

AIM: Assembly Language Programming

APPARATUS REQUIRED: -

Sr. no.	Name of equipments/components/software	Specification/range/rating/version	Quantiy
1	8085 Microprocessor programming kit, instruction coding sheet.	SCIENTECH-8085	1
2.	Power supply	A.C (230V Mains)	1

DESCRIPTION/ALGORITHM:-

Write a program to add two hexadecimal & decimal numbers.

- **HEXADECIMAL ADDITION :**The program takes the content of 2009, adds it to 200B & stores the result back at 200C.

Steps : 1. Initialize HL Reg. pair with address where the first number is lying.

2. Store the number in accumulator.

3. Get the second number.

4. Add the two numbers and store the result in 200B.

5. Go back to Monitor

Let: (2009 H) = 80 H

(200B H) = 15 H

Result = 80 H + 15 H = 95 H

(2009 H) A →

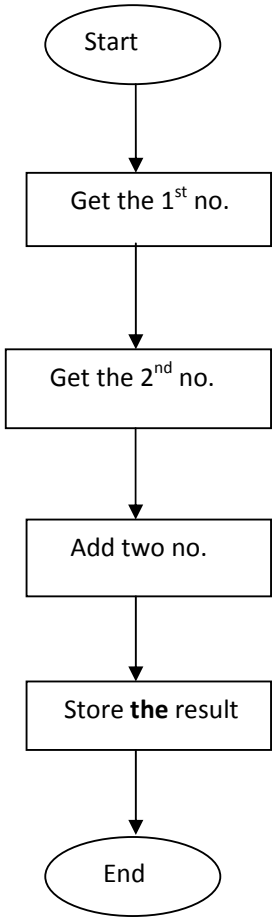
A B →

(200B H) → A

A + B A →

A → (200C H)

FLOWCHART : -



PROGRAM:-

LXI H, 2009 ; Point 1st no.

MOV A, M ; Load the acc.

```
INX H       ;    Adv Pointer
ADD M       ;    ADD IIND NO.
INX H       ;    Adv Pointer
MOV M, A    ;    Store Result
RST 5       ;
```

- **DECIMAL ADDITION:**

Steps: 1. Initialize HL Reg. pair with address where the first number is lying.

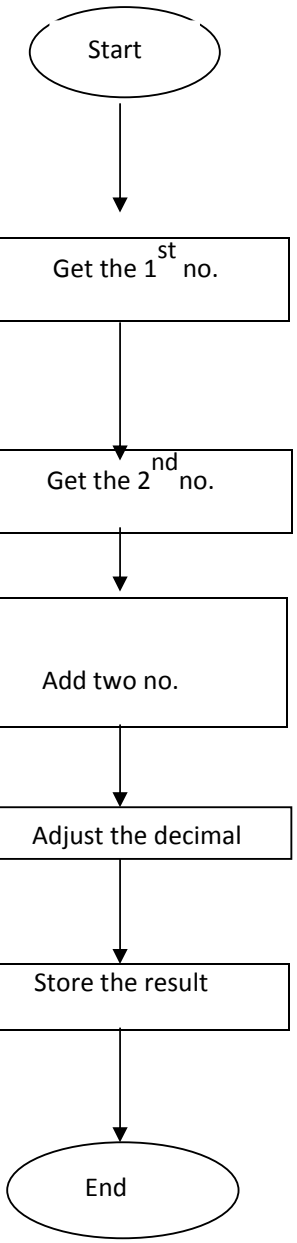
2. Store the number in accumulator.

3. Get the second number.

4. Add the two numbers and store the result in 200B.

5. Go back to Monitor

FLOWCHART:-


Start
Get the 1st no.
Get the 2nd no.
Add two no.
Adjust the decimal
Store the result
End

PROGRAM:-

```
LXI H, 2009     ;       Point 1st no.
        MOV A, M        ;       Load the acc.
        INX H           ; Adv Pointer
        ADD M           ;       ADD IIND NO.
        DAA     ;       Adjust the decimal
        INX H           ;       Adv Pointer
        MOV M, A        ;       Store Result
        RST 5
```

RESULTS:- Results are verified

1) **How many machine cycles required to excute add instruction?**
2) **What is the function of DAA instruction?**
3) **What is the importance of stack pointer?**
4) **How many bites of instruction is** MOV M, A