ELECTRONICS ENGINEERING II LAB

MANUAL

EEC -451

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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SYLLABUS FOR ELECTRONICS ENGINEERING II DESIGN LAB

EEC -451: Electronics Engineering II Lab

Objective: To understand the digital logic and create various systems by using these logics.

1. Measurement of Operational Amplifier Parameters-Common Mode Gain, Differential Mode Gain, CMRR, Slew Rate.
2. Applications of Op-amp- Op-amp as summing amplifier, Difference amplifier, Integrator and differentiator.

3. Field Effect Transistors-Single stage Common source FET amplifier –plot of gain in dB Vs frequency, measurement of, bandwidth, input impedance, maximum signal handling capacity (MSHC) of an amplifier.

4. Bipolar Transistors- Design of single stage RC coupled amplifier –design of DC biasing circuit using potential divider arrangement –Plot of frequency Vs gain in dB. Measurement of bandwidth of an amplifier, input impedance and Maximum Signal Handling Capacity of an amplifier.

5. Two stage Amplifier. Plot of frequency Vs gain . Estimation of Q factor, bandwidth of an amplifier
6. Common Collector Configuration-Emitter Follower (using Darlington pair)-Gain and input impedance measurement of the circuit.

7. Power Amplifiers-Push pull amplifier in class B mode of operation –measurement of gain.

8. Differential Amplifier –Implementation of transistor differential amplifier .Non ideal characteristics of differential amplifier.

9. Oscillators -Sinusoidal Oscillators- (a) Wein bridge oscillator (b) phase shift oscillator.
10. Simulation of Amplifier circuits studied in the lab using any available simulation

STUDY AND EVALUATION SCHEME

SESSIONAL EVALUATION:-

CLASS TEST	**:**	**10 MARKS**
TEACHER'S ASSESMENT	**:**	**10 MARKS**
EXTERNAL EXAM	**:**	**30 MARKS**
TOTAL	**:**	**50 MARKS**

EEC-451 ELECTRONICS ENGINEERING LAB II

1. **Measurement of operational amplifier parameters**- Common Mode Gain, Differential Mode Gain, CMRR, Slew Rate.
2. **Applications of OP-amp**- OP-amp as summer amplifier, difference amplifier, integrator and differentiator.
3. **Field effect Transistors**- Single stage common source FET amplifier-plot of gain in dB Vs frequency, measurement of bandwidth, input impedance maximum signal handling capacity (MSHC) of an amplifier.
4. **Bipolar transistors**: Design of single stage RC coupled amplifier-design of DC biasing circuit using potential divider arrangement- plot of frequency Vs gain in dB. Measurement of bandwidth of an amplifier, input impedance and Maximum Signal Handling Capacity of an amplifier.
5. **Two stage Amplifier:** Plot of frequency Vs gain. Estimation of Q factor, bandwidth of an amplifier.
6. **Common Collector Configuration - Emitter Follower (**using Darlington pair**):** Gain and input impedance measurement of the circuit.
7. **Power Amplifiers :** Push pull amplifier in class B mode of operation- measurement of gain.
8. **Differential Amplifier:** Implementation of transistor differential amplifier. Non ideal characteristics of differential amplifier.
9. **Oscillators:** Sinusoidal Oscillators- (a) Wein bridge oscillator (b) phase shift oscillator.
10. **Simulation of Amplifier:** circuits studied in the lab using any available simulation software and measurement of bandwidth and other parameters with the help of simulation software.

EXPERIMENT NO 1

AIM:- Measurement of operational Amplifier Parameters – Common Mode Gain, Differential Mode Gain, CMRR, Slew Rate.

EQUIPMENT REQUIRED:

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	multimeter		1	
4.	CRO		1	

THEORY:

1. **Common Mode Gain**: When the same input voltage is applied to both input terminals of an op-amp the op-amp is said to be operating in common mode operation, since the input
2. voltage applied is common to both the inputs, it is referred as common mode voltage v_{cm} . A common mode voltage v_{cm} can be ac, dc or a combination of ac and dc.

$$V_i = \frac{V_1+V_2}{2}$$

$$V_{ocm}=A_{cm}XV_i$$

$$\mathbf{A_{cm}= \frac{V_{ocm}}{V_i}}$$

3. **Differential Mode Gain** :

$$V_o \approx (V_1-V_2) \qquad \text{(For ideal op-amp)}$$

$$V_o=A_d(V_1-V_2)$$

$$\mathbf{A_d= \frac{V_o}{}}$$

$$\mathbf{V_1\text{-}V_2}$$

Where, V_d: Differential voltage

$$V_d = V_1\text{-}V_2$$

$$\mathbf{A_d = \frac{V_o}{V_d}}$$

Total Output

$$\mathbf{V_o = A_d V_d + A_{cm} V_{cm}}$$

4. **Common mode Rejection Ratio (CMRR)**: The ability of the op-amp to reject the signal on both terminals such as noise is called as CMRR. Ideally gain of common mode is zero ,hence the ideal value of CMRR is∞..Mathematically it is the ratio of the Differential Gain to common mode gain.

$$\mathbf{CMRR = A_d/A_{cm}}$$

Where, A_d =differential gain

A_{cm} = common mode gain.

$$\mathbf{CMRR\ in\ dB = 20 \log A_d/A_{cm}}$$

5. **Slew Rate**: Slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is specified in V/μs.

$$V_s = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t$$

$$d/dt\ V_o = V_m\ \omega \cos \omega t$$

But, Slew rate $S = Vo\ d/dt\ I_{max.}$

Put max value of Cos ω t in the equation

$$S = Vm\ \omega \qquad (\omega = 2\pi f)$$

$$\mathbf{S = Vm\ 2\pi f\ v/sec}$$

PROCEDURE:

A. Common Mode Rejection ratio (CMRR) :

(1) Connect the circuit as shown in fig (a) to measure differential gain.

(2) Apply V_1 and V_2 inputs.

(3) Measure the output voltage, find differential gain.

(4) Connect the circuit as shown in fig (b) to measure common mode gain.

(5) Apply input and measure output voltage, find common mode gain.

(6) Find CMRR.

B. Slew Rate :

(1) Connect the opamp as shown in circuit.

(2) Adjust the sine wave signal generator so that the output 1V sine wave at 1k H_z.

(3) Slowly increase the input signal frequency until the output gets just distorted.

(4) Calculate slew rate, SR =2*3.14*F $V_{m/10}{}^{6}$ v/us

(5) Increase the input freq slowly until the output is just barely a triangular wave.

The slew rate SR = change in the output voltage amplitude. v/us

change in the output time

PRECAUTION:

(1) Do not connect more than 15 V to the op amp.

(2) The wires should be connected properly to the bread board.

(3) Measurement should be taken properly.

PRE EXPERIMENTAL QUESTIONS:

Q. Define Opamp.

A. An operational amplifier ("op-amp") is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output.[1] An op-amp produces an output voltage that is typically hundreds of thousands times larger than the voltage difference between its input terminals.

Q. What are the ideal characteristics of OpAmp?

A. Ideal op-amps characteristics

An equivalent ircuit of an operational amplifier that models some resistive non-ideal parameters.

An ideal op-amp is usually considered to have the following properties, and they are considered to hold for all input voltages:

Infinite open-loop gain (when doing theoretical analysis, a limit may be taken as open loop gain AOL goes to infinity).
Infinite voltage range available at the output () (in practice the voltages available from the output are limited by the supply voltages). The power supply sources are called rails.

Infinite bandwidth (i.e., the frequency magnitude response is considered to be flat everywhere with zero phase shift).

Infinite input impedance.

Zero input current (i.e., there is assumed to be no leakage or bias current into the device).

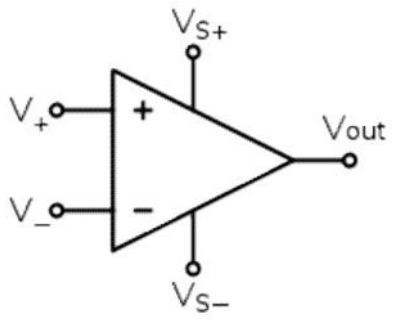
Zero input offset voltage (i.e., when the input terminals are shorted so that , the output is a virtual ground or).
Infinite slew rate (i.e., the rate of change of the output voltage is unbounded) and power bandwidth (full output voltage and current available at all frequencies).

Zero output impedance (i.e., , so that output voltage does not vary with output current).
Zero noise.

Infinite Common-mode rejection ratio (CMRR).

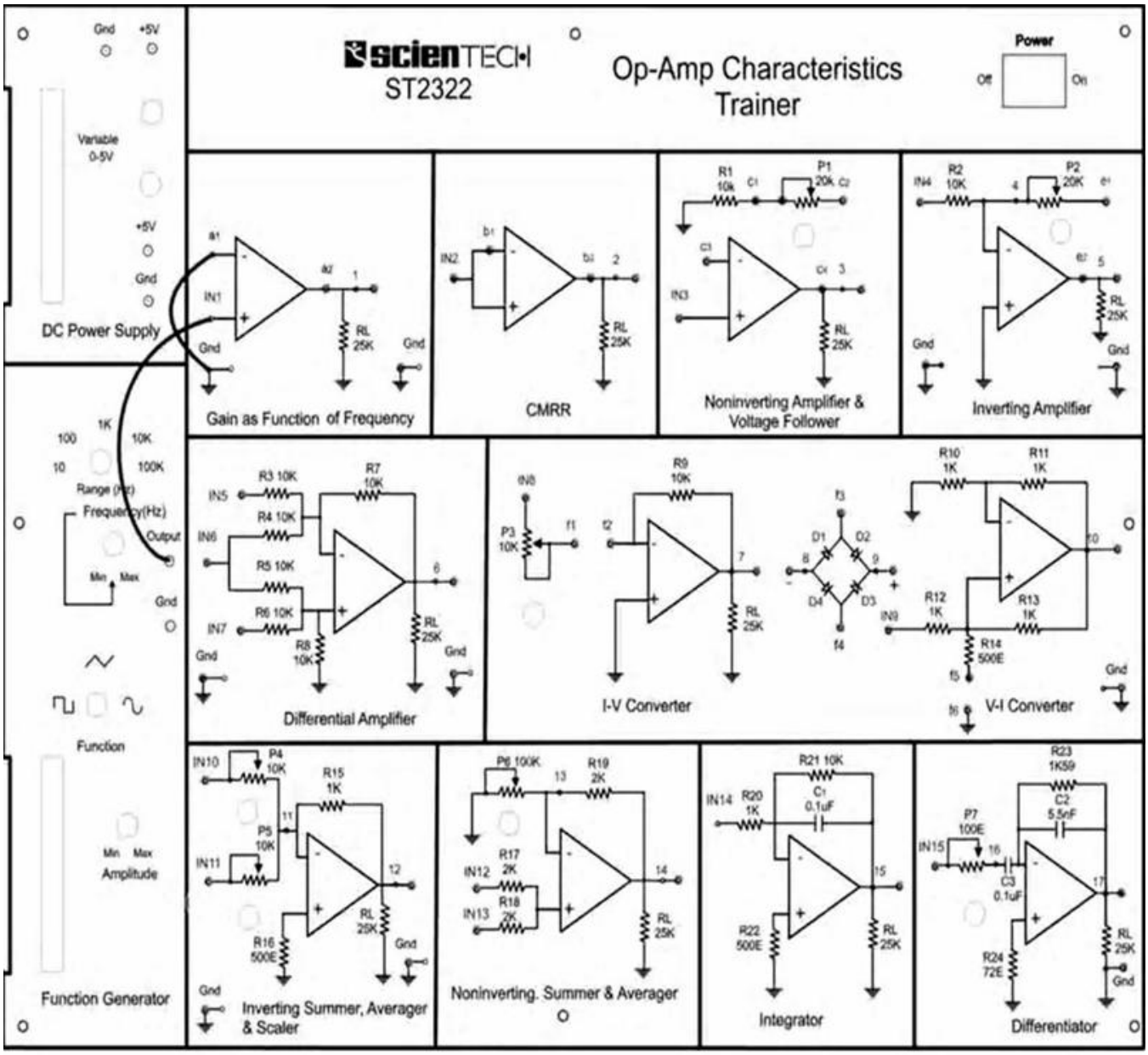
Infinite Power supply rejection ratio for both power supply rails.

Q. Draw the symbol of OpAmp.
A.



POST EXPERIMENTAL QUESTIONS:

Q. What are the applications of Opamp?
A. audio- and video-frequency pre-amplifiers and buffers, differential amplifiers, differentiators and integrators, filters, precision rectifiers, precision peak detectors, voltage and current regulators, analog calculators, analog-to-digital converters, digital-to-analog converters, voltage clamps, oscillators and waveform generators


scienTECH
ST2322
Op-Amp Characteristics Trainer
Power
Off
On
Gnd
+5V
Variable 0-5V
DC Power Supply
Gain as Function of Frequency
CMRR
Noninverting Amplifier & Voltage Follower
Inverting Amplifier
Differential Amplifier
I-V Converter
V-I Converter
Function
Amplitude
Function Generator
Inverting Summer, Averager & Scaler
Noninverting. Summer & Averager
Integrator
Differentiator

EXPERIMENT NO.2

AIM:-Applications of Op-amp - Op-amp as summing amplifiers, Difference amplifier, Integrator and differentiator.

EQUIPMENT REQUIRED:

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	multimeter		1	
4.	CRO		1	

THEORY:

(1) SUMMING AMPLIFIER: The summing circuit using Op-amp as inverting mode configuration with three inputs V_a ,V_b,V_c is shown in fig. This circuit acts as a summing amplifier that means at the output we get addition of the three inputs according to the circuit given in figure. Output equation is given as

$$V_A = V_B = 0V$$

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1}$$

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2}$$

$$I = \frac{V_A - V_0}{R_f} = \frac{-V_o}{R_f}$$

Using KCL

$I=I_1+I_2$

$$\frac{-V_O}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2}$$

$$\frac{-V_O}{R_f} = \frac{V_1 + V_2}{R_1} \qquad \text{If } R_1=R_2$$

$$V_O = -\frac{R_f}{R_1}(V_1 + V_2)$$

$$\mathbf{V_O=-R_f/R_1\,(V_1+V_2)}$$

(2) **<u>DIFFERENCE AMPLIFIER</u>:** Difference circuit using Op-amp is shown in fig. This circuit act as a difference means when the input V_a and V_b is give at two terminals as shown in the circuit then the output at output terminals is the difference of the two input. Theoretical equation is given as

$$\mathbf{V_o = R_f/R_1\,(V_2-V_1)}$$

(3) **<u>INTEGRATOR</u>:** Output of the integral of the input with scale multiple of 1/RC. This Property to integrate a given signal provides the ability to electrically solve analogs of physical system operation.

$$V_A = V_B = 0V$$

$$I = \frac{V_{in}-V_A}{R1} = \frac{V_{in}}{R1}$$

$$I_1 = Cf\,\frac{d(V_A-V_O)}{dt} = -Cf\,\frac{dV_O}{dt}$$

$$I_2 = \frac{V_A-V_O}{R_f} = \frac{V_O}{R_f}$$

At node A using KCL

$$I=I1+I2$$

$$\frac{V_{in}}{R_1} = -\frac{Cf\,dV_O}{dt} + \frac{(-V_O)}{Rf}$$

Taking Laplac

$$\frac{Vin\,(s)}{R1} = -sCf\,V_O(S) - \frac{V_Os}{Rf}$$

$$\frac{Vin\,(s)}{R1} = -VO(s)\left(sCf + \frac{1}{Rf}\right)$$

$$\frac{Vin\ (s)}{R1} = -VO(s)\left(sCf\ Rf + \frac{1}{Rf}\right)$$

$$\frac{-\ Rf}{(sCf + 1)\ R1}\ Vin\ (s) = VO(s)$$

When Rf is very large then R_1/Rf is neglecte hence the circuit behave like an ideal integrtor.

$$V_O(s) = - \frac{1}{(sCf\ Rf + R1\ /\ Rf)} Vin\ (s)$$

$$\mathbf{V_O(s) = - \frac{1}{(sCf\ Rf)}\ Vin\ (s)}$$

$$\text{i.e. } \mathbf{V_O(t) = -1\ \frac{\int Vin(t)\ dt}{R1Cf}}$$

(4) <u>DIFFERENTIATOR:</u> Output is differential of input with a scale factor of RC

$$\mathbf{Vo\ (t) = -RC\ \frac{dvi(t)}{dt}}$$

<u>PROCEDURE</u>:

(a) Connect the circuit as shown in the figure.

(b) Check all the continuity to proper connection.

(c) Apply voltages to all input.

(d) Measure the output by the CRO.

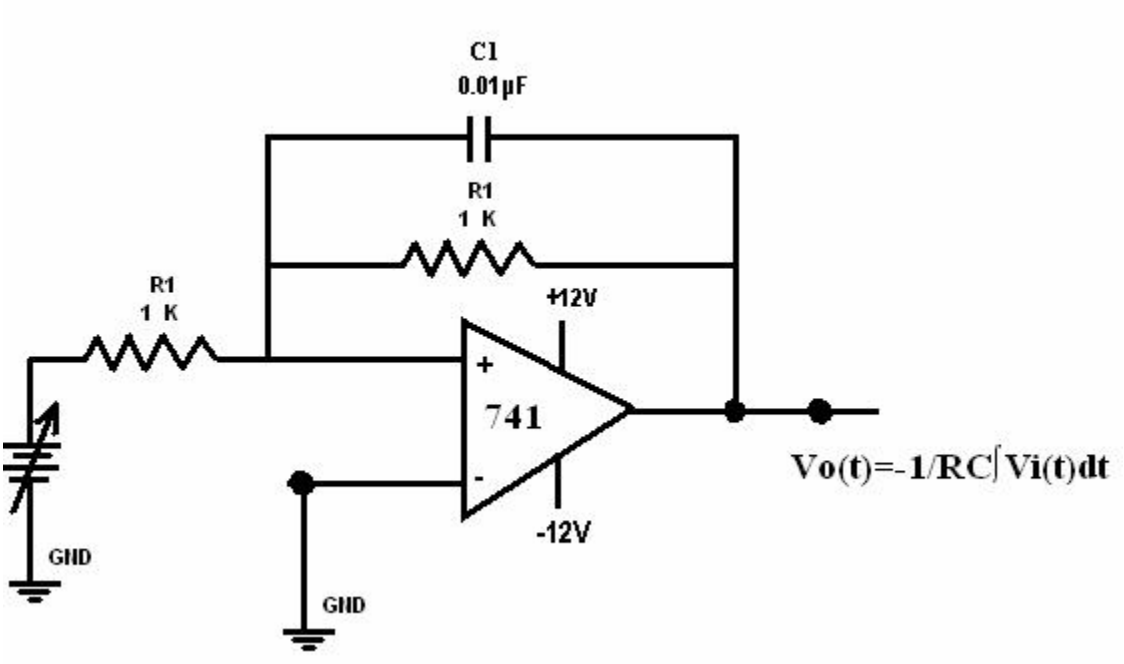
(e) Verify this output with theoretical equation.

<u>PRECAUTIONS:</u>

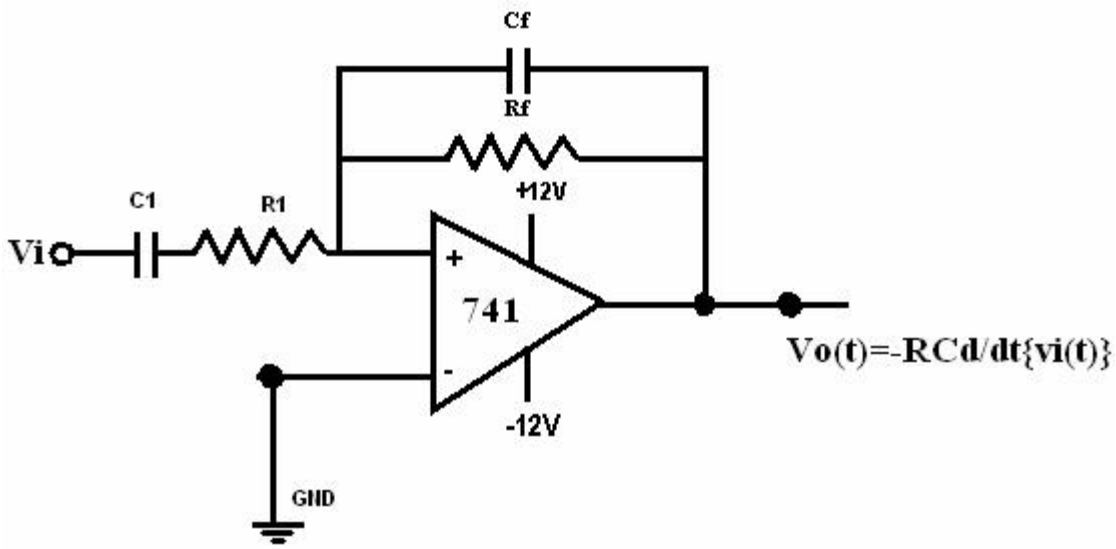
(a) Do not connect more than 15 V to the op amp.

(b) The wires should be connected properly to the bread board.

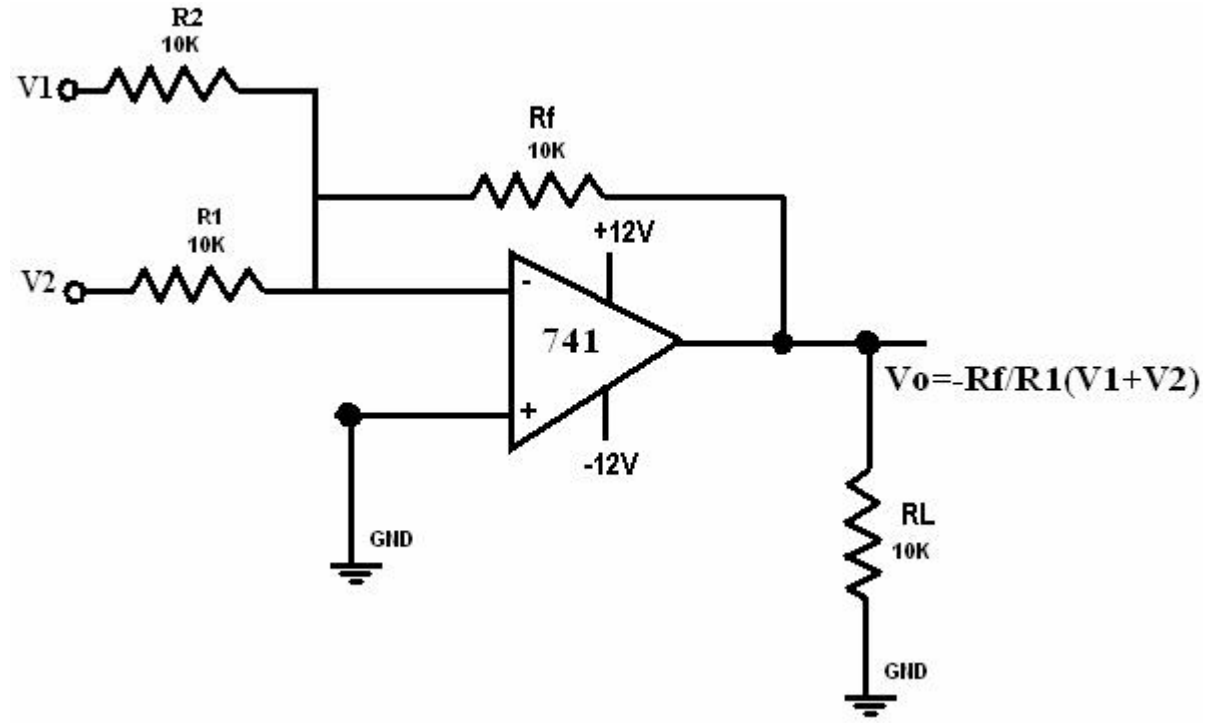
(c) Measurement should be taken properly.



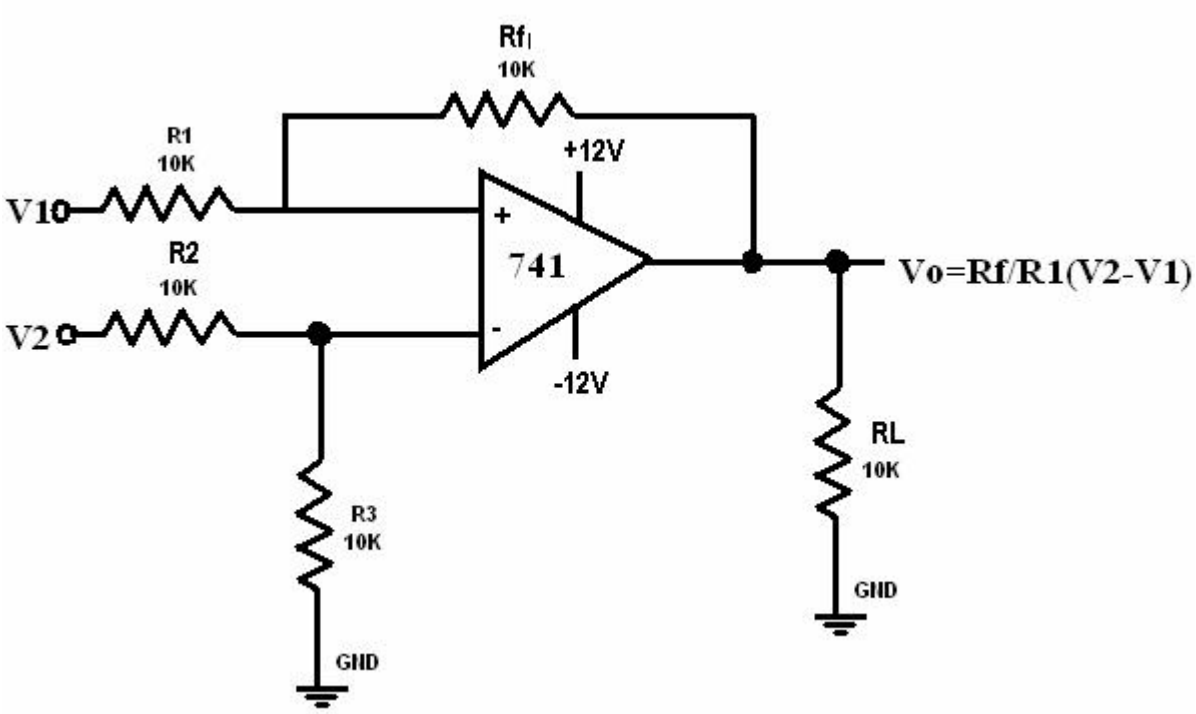
Integrator Amplifier



Differentiator Amplifier



Summer Amplifier



Difference Amplifier

PRE EXPERIMENTAL QUESTIONS:

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A. Ideal op-amps characteristics

An equivalent ircuit of an operational amplifier that models some resistive non-ideal parameters. An ideal op-amp is usually considered to have the following properties, and they are considered to hold for all input voltages:

Infinite open-loop gain (when doing theoretical analysis, a limit may be taken as open loop gain AOL goes to infinity).

Infinite voltage range available at the output () (in practice the voltages available from the output are limited by the supply voltages). The power supply sources are called rails.

Infinite bandwidth (i.e., the frequency magnitude response is considered to be flat everywhere with zero phase shift).

Infinite input impedance (so, in the diagram, , and zero current flows from to).

Zero input current (i.e., there is assumed to be no leakage or bias current into the device).

Zero input offset voltage (i.e., when the input terminals are shorted so that , the output is a virtual ground or).
Infinite slew rate (i.e., the rate of change of the output voltage is unbounded) and power bandwidth (full output voltage and current available at all frequencies).

Zero output impedance (i.e., , so that output voltage does not vary with output current).
Zero noise.

Infinite Common-mode rejection ratio (CMRR).

Infinite Power supply rejection ratio for both power supply rails.

Q. Draw the symbol of OpAmp.
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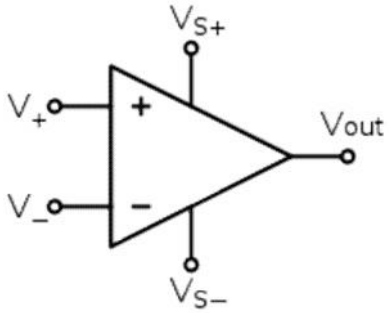
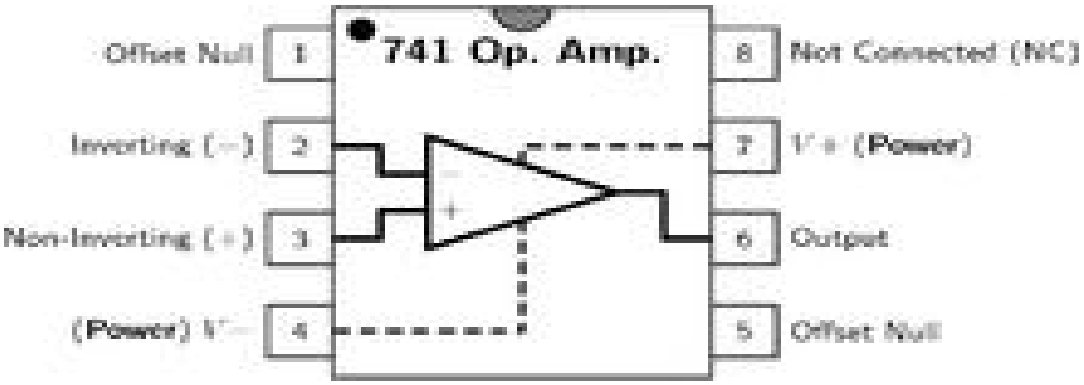


POST EXPERIMENTAL QUESTIONS:

Q. Draw the pin diagram of OpAmp .

A.



Q. What are the applications of Opamp?

A. audio- and video-frequency pre-amplifiers and buffers, differential amplifiers, differentiators and integrators, filters, precision rectifiers, precision peak detectors, voltage and current regulators, analog calculators, analog-to-digital converters, digital-to-analog converters, voltage clamps, oscillators and waveform generators

EXPERIMENT NO 3

AIM:- **FIELD EFFECT TRANSISTORS: -** Single stage common source FET amplifier-plot of gain in db V_s frequency, measurement of, bandwidth, input impedance, maximum signal handling capacity (MSHC) of an amplifier.

EQUIPMENT REQUIRED:-

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	multimeter		1	
4.	CRO		1	

CRO, Signal generator, Power Supply, Bread-board, Resistors (1MΩ, 4.7KΩ, 1KΩ), Capacitors (10μF, 100Mf), FET-BFW10 and connecting Wires.

THEORY:-

A JFET can be N-channel type or P-channel type. The structure of a P-channel JFET is similar to that of an N-channel JFET. Except that in its structure, N-type is replaced by P-type and P-type by N-type. The structure of an N-channel JFET is abar of N-type silicon. This bar behaves like a resistor between its two terminals, called source and drain. We introduce heavily doped P-type region on either side of bar. These P-regions are called gates. Usually two gates are connected together. This gate is used to control current flow from source to drain. This flow of electrons makes the drain current I_d. The electrons in the bar pass through the space between the two P-regions. As width of this space between the p-regions can be controlled by varying gate voltage that is called a channel. We apply a small reverse bias to the gate. Because of the reverse bias, the width of depletion increases. Since the N-type bar is lightly doped compared to the P-regions, the depletions region extends more into the N-type bar. This reduced the width of the channel. Reduction in the width of the channel (the conductive portion of the bar) increases its resistance. This reduces the drain current I_d. There is one important point about the channel shape. It is narrower at the drain end. This happens because the amount of reveres bias is not same throughout the length of the P-N junction. When current flows through the bar, a potential drop occurs across its length. As a result

the reverse bias between the gate and the drain end of the bar is more than that between the gate and the source end of the bar. The width of depletion region is more at the drain end than at the source end. As a result, the channel becomes narrower at the drain end. If the reverse gate bias is increased further, the channel becomes narrower at the drain end and drain current further reduces. If the reverse bias is made sufficiently large, the depletion region will extend into channel. This pinches off all current flow. The gate-source voltage at which pinch-off occurs is called PINCH-OFF voltage V_p.

PROCEDURE:-

(1) Connect the circuit as per the circuit diagram.

(2) Apply V_i = 10 mV and V_{dd} = +20v.

(3) Now vary the frequency of the input signal and measure the corresponding amplitude variation in output at different values frequency.

(4) Note down the readings and plot the graph between gain and frequency. This curve is known as frequency response curve.

OBSERVATIONS:-

S. NO	INPUT VOLTAGE (V_i)	INPUT FREQUENCY (F_i)	OUTPUT VOLTAGE (V_o)	GAIN (db)

RESULT:-

Thus we have plotted a graph between gain and frequency to obtain a frequency response curve. The values of f_L and f_H from graph are given as

F_H =

F_L =

$BW = F_H - F_L$

PRECAUTIONS:-

(1) All connections should be right and tight.

(2) Readings should be taken carefully.

(3) Scale on the graph should be taken correctly and carefully.

PRE EXPERIMENTAL QUESTIONS:

Q. Define FET.

A. The **field-effect transistor** (FET) is a transistor that uses an electric field to control the shape and hence the conductivity of a channel of one type of charge carrier in a semiconductor material. FETs are sometimes called *unipolar transistors* to contrast their single-carrier-type operation with the dual-carrier-type operation of bipolar (junction) transistors (BJT). The *concept* of the FET predates the BJT, though it was not physically implemented until *after* BJTs due to the limitations of semiconductor materials and the relative ease of manufacturing BJTs compared to FETs at the time.

Q. What are different terminals of FET?

A. The FET's three terminals are:

Source (S), through which the majority carriers enter the channel. Conventional current entering the channel at S is designated by I_S.

Drain (D), through which the majority carriers leave the channel. Conventional current entering the channel at D is designated by I_D. Drain to Source voltage is V_{DS}.

Gate (G), the terminal that modulates the channel conductivity. By applying voltage to G, one can control I_D

POST EXPERIMENTAL QUESTIONS:

Q. What are advantages of the FET.

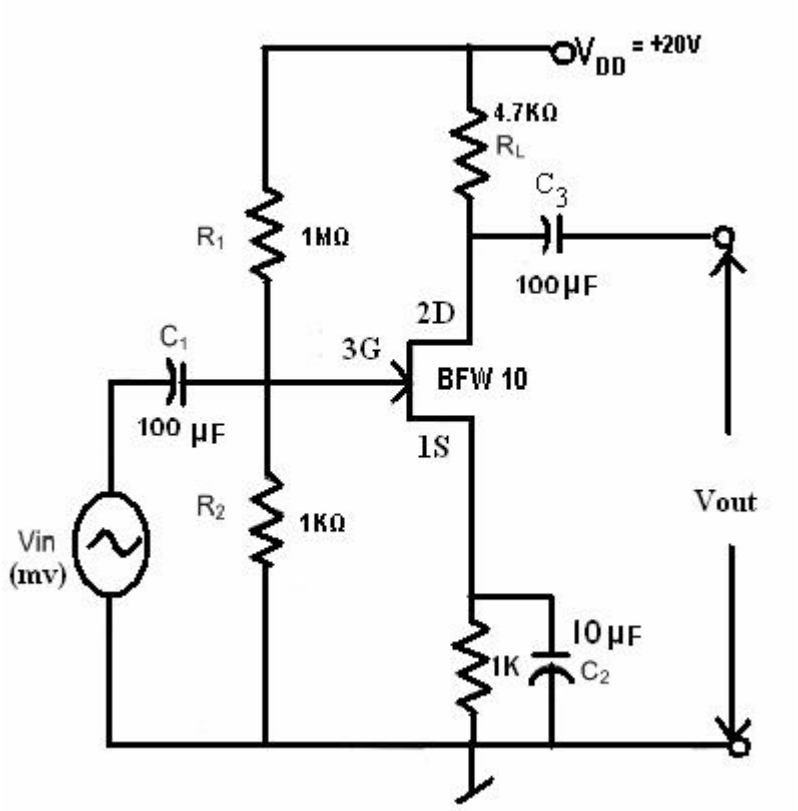
A. The main advantage of the FET is its high input resistance, on the order of 100M ohms or more. Thus, it is a voltage-controlled device, and shows a high degree of isolation between input and output. It is a unipolar device, depending only upon majority current flow. It is less noisy and is thus found in FM tuners for quiet reception. It is relatively immune to radiation. It exhibits no offset voltage at zero drain current and hence makes an excellent signal chopper. It typically has better thermal stability than a BJT.

Q. What are disadvantages of the FET?

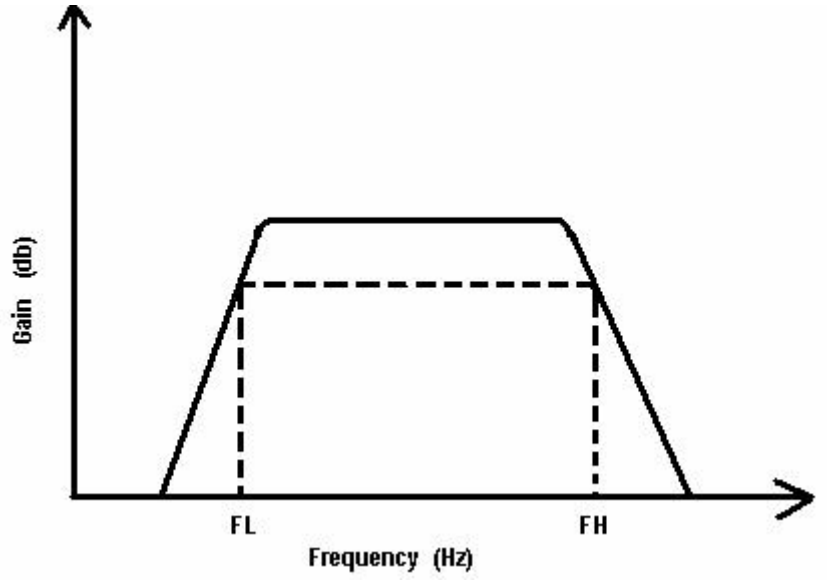
A. It has relatively low gain-bandwidth product compared to a BJT. The MOSFET has a drawback of being very susceptible to overload voltages, thus requiring special handling during installation.

Q. What are the various applications of FET?

A. Applications are in switching internal combustion engine ignition coils, where fast switching and voltage blocking capabilities are important.
The most commonly used FET is the MOSFET. The CMOS (complementary metal oxide semiconductor) process technology is the basis for modern digital integrated circuits. This process technology uses an arrangement where the (usually "enhancement-mode") p-channel MOSFET and n-channel MOSFET are connected in series such that when one is on, the other is off.



Single Stage RC Coupled FET Amplifier



Frequency Response

EXPERIMENT NO - 4

AIM :- **Bipolar transistor**:- Designing of single stage RC coupled amplifier-design of DC biasing circuit using potential divider arrangement – plot of frequency V_s gain in db. Measurement of bandwidth of an amplifier, input impedance and Maximum signal Handing Capacity of an amplifier.

APPARATUS:-

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	multimeter		1	
4.	CRO		1	

CRO, Power supply, Signal Generator, Bread-board, Resistors, capacitors ,transistor (BC 107) and connecting wires.

Design of RC coupled amplifier (DC biasing circuit design)

Design values: design a voltage divider circuit for given values:

$I_C = 2mA$ $V_{CE} = 4V$

$R_C = 2K\Omega$ $V_{CC} = 10V$

Determine the values of R_1, R_2,and R_E.

Solution:

$$Ic = \beta I_B$$

$$I_B = \frac{Ic}{\beta}$$

$$I_1 = 10 \text{ X } I_B$$

$$I_1 = \frac{VCC}{R_1+R_2}$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad .....(I_C = I_E)$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$Ic = \frac{V_B - V_{BE}}{R_E}$$

$$V_B = I_C \times R_E$$

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

THEORY: Almost no electronic system can work without an amplifier. The voice of a single person could reach everybody in a hall only because of the amplification of the signal picked up by the P.A system. After a transistor is biased in the active region, it can work as an amplifier. We apply an ac voltage between the base and emitter terminals to produce fluctuations in the collector current .An amplified output signal is obtained when this fluctuating collector current flows through a collector resistor R_c.When the input signal is so weak as to produce small fluctuations in the collector current compared to its quiescent value, the amplifier is called 'small signal amplifier' (also 'voltage amplifier'). Such an amplifier is used as the first stage of the amplifier used in receivers (radio and TV), tape recorders, and stereos and measuring instruments.The circuit of a single stage transistor amplifier is shown in fig. Almost all amplifiers use potential divider biasing circuit because the design of the circuit is simple and it provides good stabilization of the operating point. If this circuit is to amplify ac voltages, some more components must be added such as the circuit capacitors are added. The capacitor C_C is called coupling capacitors. A coupling capacitor passes an ac signal from one side to another. The capacitor C_E works as a bypass capacitor. It bypasses all the ac currents from the emitter to ground. The resistance R represents the resistance of whatever is connected at the output. To what extent an amplifier enlarges signal is expressed in terms of its voltage gain. The voltage gain of an amplifier is given as –

A_V = output AC voltage / input AC voltage

$A_V = V_o/V_i$

The other quantities of interest for a voltage amplifier are current gain (A_i) input impedance (z_i) and output impedance (z_o).The performance of an amplifier is judged by observing whether all frequency component of the signal are amplified equally well. The information is provided by its frequency response curve. This curve illustrates how the magnitude of voltage gain of the amplifier varies with the freq. of the input signal (sinusoidal). It can be plotted by measuring voltage gain of the amplifier

for different frequencies of sinusoidal voltage fed to its input. Fig shows the frequency response curve of the typical RC coupled amplifier.

$$B.W = f_2 - f_1$$

PROCEDURE:-

(1) Connect the circuit as the cat. Diagram.

(2) Apply V_{cc} = +15V &set i/p voltage in mV.

(3) Now vary the frequency of i/p voltage &Measure the corresponding amplitude variation in o/p at different values of i/p frequency.

(4) Not down the reading and plot a graph between gain and frequency. The curve is known as frequency response curve.

OBSERVATIONS:-

S. NO	**Input Voltage (V_i)**	**Input Frequency (f)**	**Output Voltage (V_O)**	**Gain $A=20\log_{10}(V_o/V_i$**

RESULT:- Thus we have plot a graph between gain and frequency. This curve is known as frequency response curve and values of f2 and f1 from graph are:-

F_H = F_L =

B.W = Z_i =

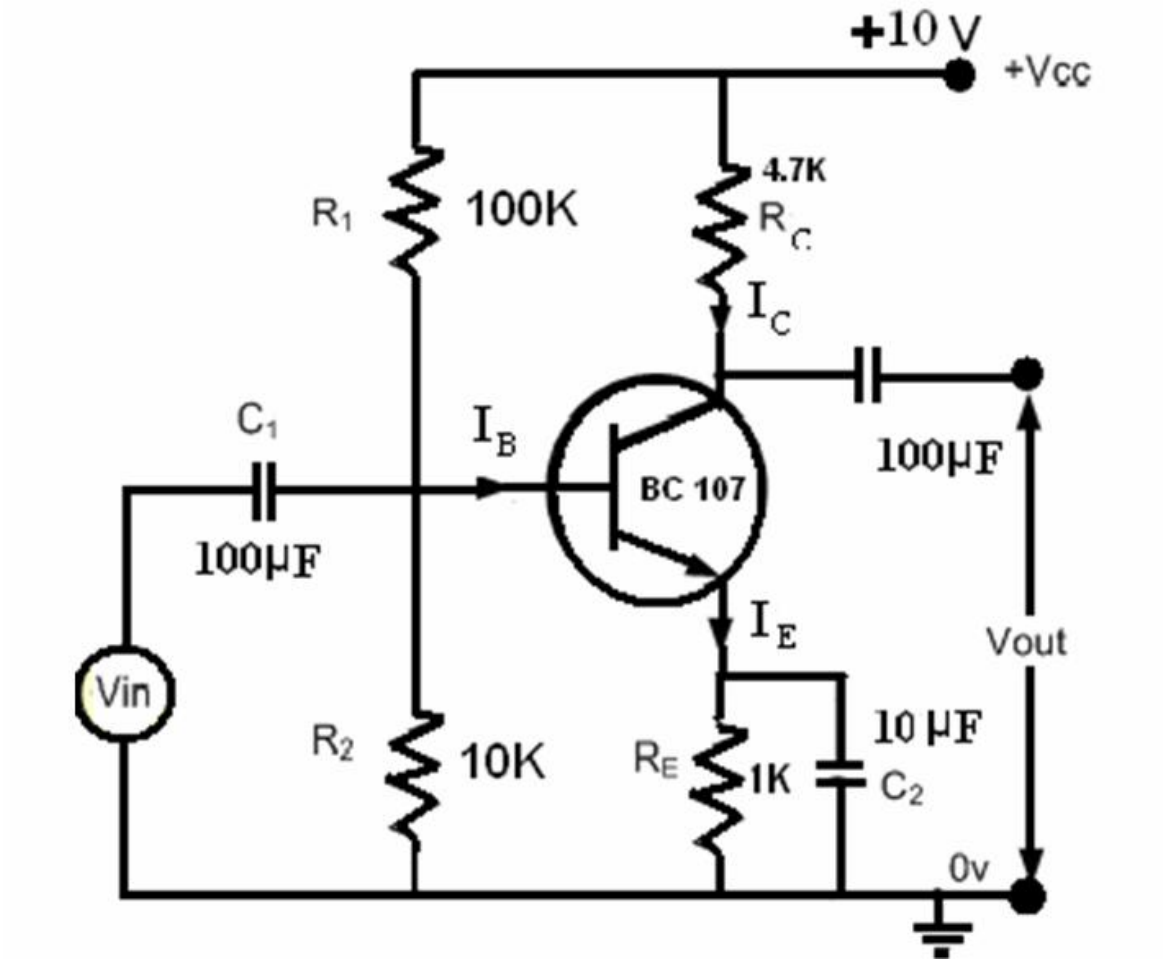
Max signal handling capacity =

PRECAUTIONS:-

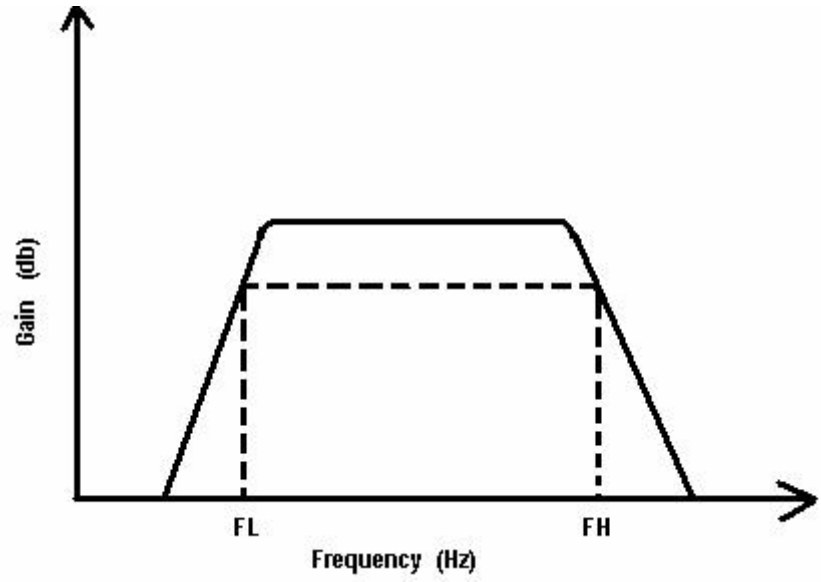
(1) All connection should be right & tight.

(2) Readings should be taken carefully.

(3) Scale on the graph should be taken correctly & carefully.



Single Stage RC Coupled BJT Amplifier



Frequency Response PRE EXPERIMENTAL QUESTIONS:

Q. Define transistor.
A. A transistor is a semiconductor device used to amplify and switch electronic signals and electrical power. It is composed of a semiconductor material with at least three terminals for connection to an external circuit.

Q. Describe the operation of transistor as switch.

A. Transistors are commonly used as electronic switches, both for high-power applications such as switched-mode power supplies and for low-power applications such as logic gates.

In a grounded-emitter transistor circuit, such as the light-switch circuit shown, as the base voltage rises, the base and collector current rise exponentially. The collector voltage drops because of the collector load resistance (in this example, the resistance of the light bulb). If the collector voltage were zero, the collector current would be limited only by the light bulb resistance and the supply voltage. The transistor is then said to be *saturated* - it will have a very small voltage from collector to emitter. Providing sufficient base drive current is a key problem in the use of bipolar transistors as switches. The transistor provides current gain, allowing a relatively large current in the collector to be switched by a much smaller current into the base terminal. The ratio of these currents varies depending on the type of transistor, and even for a particular type, varies depending on the collector current. In the example light-switch circuit shown, the resistor is chosen to provide enough base current to ensure the transistor will be saturated.

In any switching circuit, values of input voltage would be chosen such that the output is either completely off, or completely on. The transistor is acting as a switch, and this type of operation is common in digital circuits where only "on" and "off" values are relevant.

Q. Name the ternimals of the transistor.
A. Emitter, Collector and Base.

POST EXPERIMENTALQUESTIONS:

Q. Why BJT Call as bipolar device?

A. Bipolar transistors are so named because their operation involves both electrons and holes, as opposed to unipolar transistors, such as field-effect transistors, in which only one carrier type is involved in charge flow. Although a small part of the transistor current is due to the flow of majority carriers, most of the transistor current is due to the flow of minority carriers and so BJTs are classified as minority-carrier devices.

Q. Why BJT called as current controlled device?
A. The collector–emitter current can be viewed as being controlled by the base–emitter current (current control), or by the base–emitter voltage (voltage control). These views are related by the current–voltage relation of the base–emitter junction, which is just the usual exponential current voltage curve of a PN junction (diode)

The physical explanation for collector current is the amount of minority-carrier charge in the base region. Detailed models of transistor action, such as the Gummel–Poon model, account for the distribution of this charge explicitly to explain transistor behavior more exactly. The charge-control view easily handles photo-transistors, where minority carriers in the base region are created by the absorption of photons, and handles the dynamics of turn-off, or recovery time, which depends on charge in the base region recombining. However, since base charge is not a signal that is visible at the terminals, the current- and voltage-control views are usually used in circuit design and analysis.

EXPERIMENT NO – 5

AIM:- Two Stage Amplifiers: - Plot of frequency V_s gain, Estimation of Q factor, bandwidth of an amplifier.

APPARATUS:-

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	multimeter		1	
4.	CRO		1	

C.R.O Power supply, Signal Generator, Bread – board , Resistors ,Capacitors , transistors & Connecting wires.

THEORY:- Gain of a single transistor amplifier Stage is not sufficient & has two or more stages are usually connected in cascade to provide the desired gain..

So me times cascading is done to achieve the correct I/P or O/P impedance for a specific application.

Most Popular cascade amplifier is formed by cascading several CS amplifier

Overall gain A = A1**.** A2

Where A1 & A2 are the gain of individual stages.

PROCEDURE:-

(1) Connect the circuit as per the ckt. Diagram.

(2) Apply V_{DD} =20v & set I/p voltage in mv.

(3) Now vary the frequency of I/p & measure the corresponding amplitude variation in o/p at different values of I/p frequency.

(4) Note down the reading and plot a graph between gain and frequency. The curve is known as frequency response curve.

OBSERVATION

S. NO	Input Voltage (V_i)	Input Frequency (f)	Output Voltage (V_O)	Gain $A=20\log_{10}(V_o/V_i$

RESULT:- Thus we have plot a graph between gain and frequency . This curve is known is frequency response curve and the values of f_H and f_L from graph are:-

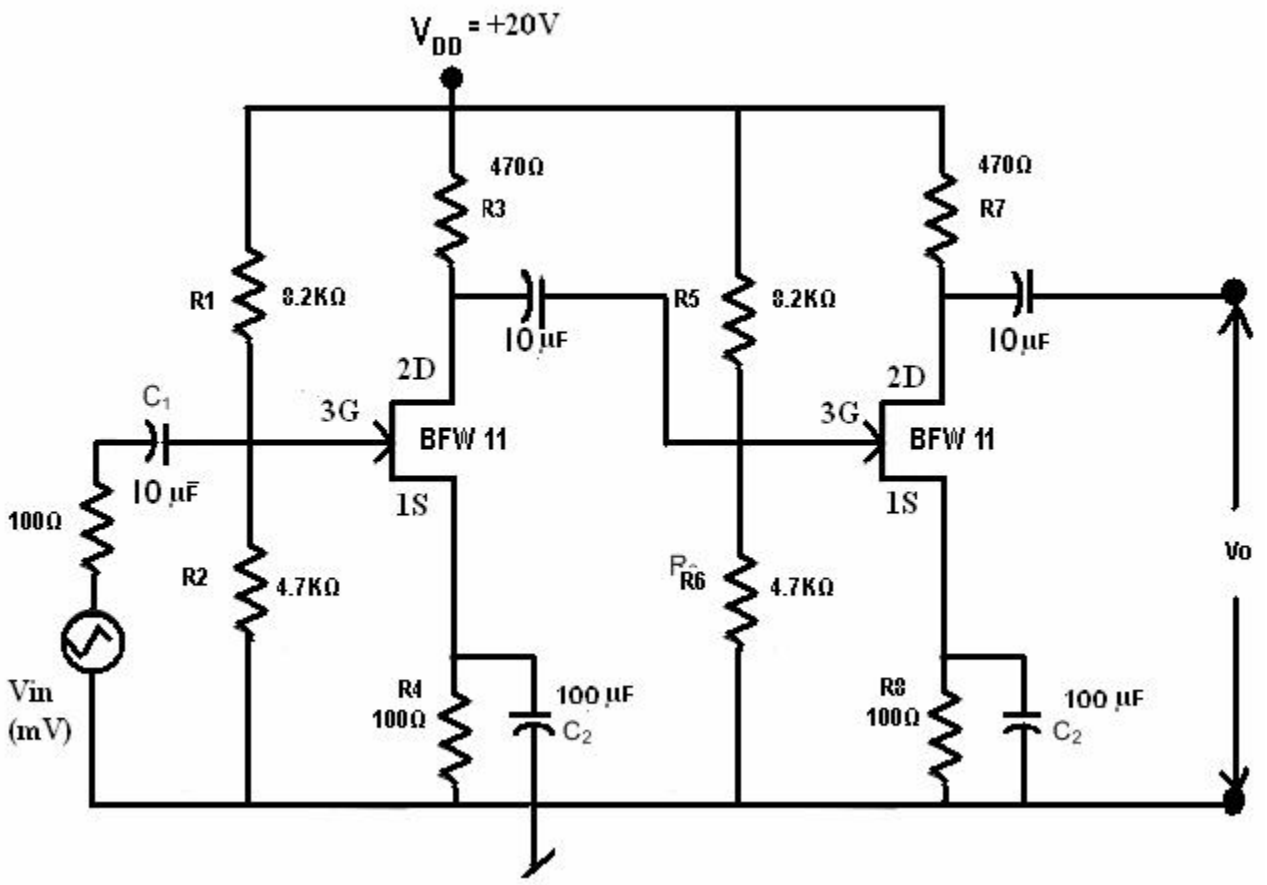
F_H = F_L = B.W =

PRECAUTION :-

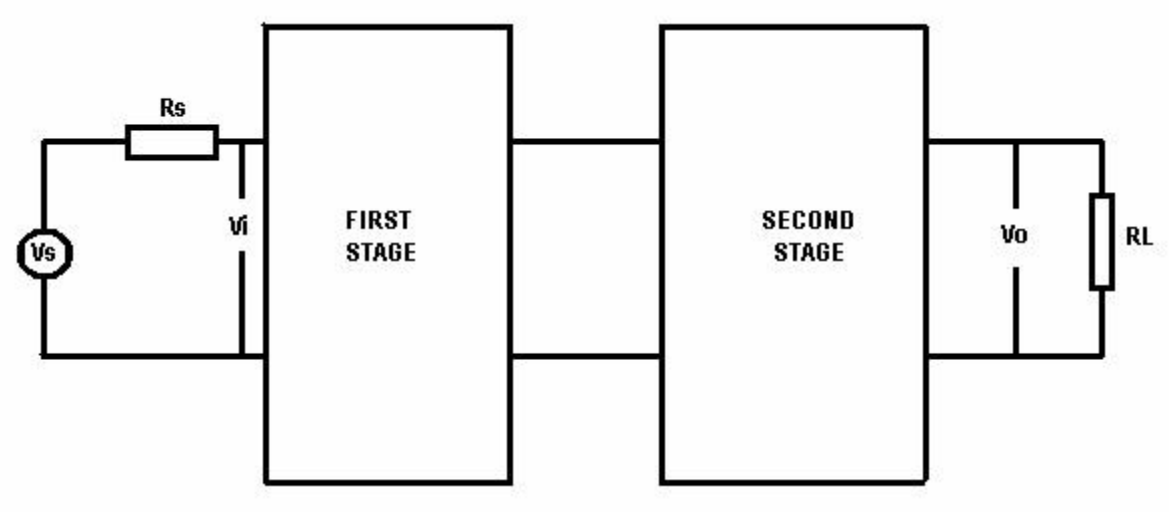
(1) All connection should be right & tight.

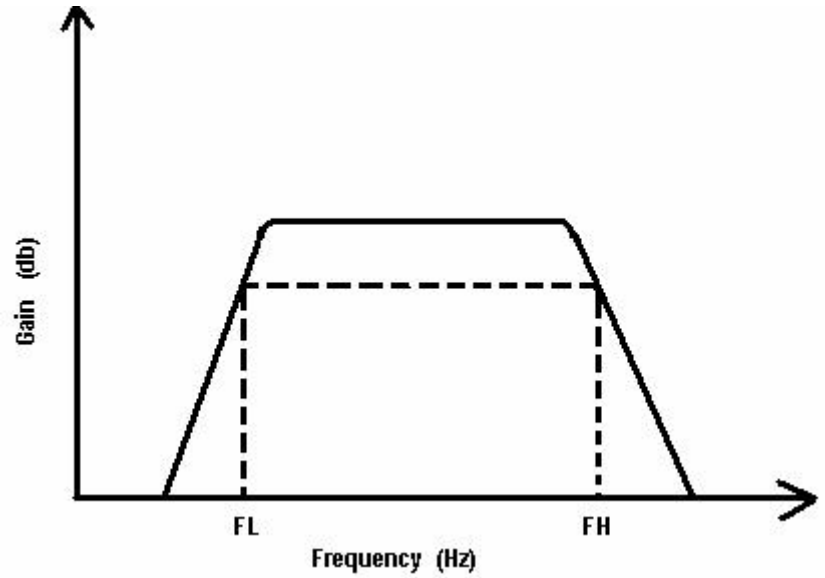
(2) Reading should be taken carefully.

(3) Scale on the graph should be taken correctly & carefully.



CASCADE CS AMLPLIFIER





FREQUENCY RESPONSE

EXPERTMENT NO -6

AIM:- Common Collector configuration-Emitter follower (using Darlington Pair):-Gain and input impedance measurement of the circuit.

APPARATUS REQUIRED:

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	multimeter		1	
4.	CRO		1	

NV6542 trainer, Digital Multimeter (DMM), Multimeter probes, 2mm Patch chords, Mains cord.

Theory:

Emitter Follower (using Darlington Pair)

In recent years, electronics have been integrated into motor speed drives and a variety of Switching-type power supplies. This means that standard discrete components needed to be altered to provide better characteristics.The need for the Darlington pair grew from the limitations of SCRs and triac-type thyristors. Thyristors control current by delaying the turn-on time. The later the pulse is applied to turn them on, the smaller the amount of current they will conduct during each cycle.On the other hand, a transistor uses variable current (0 to saturation), which provides an output current that will be a duplication of the input. This means the transistors will produce an analog signal when an analog signal is provided to its base. The simple bipolar transistor has several limitations including slow switching speeds, low gains, and larger power losses due to the switching process. A family of high-gain transistors called metal-oxide semiconductor field effect transistors (MOSFETs) was produced to address the gain problem, but they did not have the capability of controlling larger currents, so the Darlington pair was designed.The Darlington pair can actually be two discrete transistors that are connected in the driver/output configuration, or they can be a single device that has the two transistors internally connected at the point where it was manufactured as a single package. In Darlington pairs, transistor collectors are tied together and the emitter of the first transistor is directly coupled to the base of the second transistor. The total gain, which is often 1000

or more, is the- product of the gain of the individual transistors. For large currents it is standard and good procedure to use a Darlington pair of transistors, rather than a single one, which effectively acts like a single transistor with β that is the product of the two βs of the individual transistors. Figure 32 shown below is a Darlington pair since the emitter current of Q1 is the base current for Q2; the Darlington pair has an overall current gain of

$$\beta = \beta 1 \beta 2$$

ADVANTAGES:

1. The key advantage of the Darlington configuration is that the total current gain of the circuit equals the product of the current gain of two devices since its current gain is much higher
2. Darlington transistors are circuits that combine two bipolar transistors in a single device; hence, they require lesser space than configurations that use two discrete transistors.
3. Darlington connection can have very high input impedance and can produce very large outputs current.

DISADVANTAGES:

1. The disadvantage is the larger saturation voltage compared to single transistor configurations.
2. Darlington transistor pairs have more phase shift at high frequencies and can become unstable with negative feedback more easily.
3. Darlington transistors also have a higher base-emitter voltage, whiCH1s the sum of both base emitter voltages.

APPLICATIONS:

Darlington connections are used with voltage regulators and power amplifiers.

PROCEDURE FOR CURRENT GAIN , INPUT IMPEDANCE :

1. Connect a patch cord across sockets **'+12V '** of DC power supply and **'+12V '** of Emitter follower amplifier section (refer to figure 36).
2. Connect **'+5V '**of DC power supply to '$\mathbf{V_{in}}$1' terminal of Emitter follower amplifier section.
3. Connect a patch cord between socket **A** and **B** of Emitter follower amplifier section.
4. Connect a patch cord between socket **E** and **F.**
5. Now set the digital multimeter's dial to DC voltage mode.
6. Now connect the multimeter through multimeter probes to 'A' and '**G**1'.

7. Switch **on** the power supply.

8. Now measure the DC voltage between '**A'** and ground '**G1'** using DMM. This will give value of dc voltage input $\mathbf{V_{in}}$ to the transistor T1.Note it down.

9. Switch **off** the power supply.

10. Calculate the input current (Ii) by substituting the value in following equation

$$\mathbf{I_{in} = (V_{in1}-V_{in})/ Rs}$$

Where, Vin1 =5 V,Rs =100 KΩ,Vin =DC voltage measured in step 8.

11. Note down this value of input current **Ii**n.

12. Calculate the input impedance (Zin) by following formula in step 10.

$$\mathbf{Z_{in} = V_{in}/ I_i}$$

13. Now remove the patch cord between sockets '**+5**V' and '$\mathbf{V_{in1}}$'

14. Also remove the patch cord between sockets 'A' and 'B'. Connect a patch cord between socket **E** and F.

15. Now connect '**+5**V' directly at the base terminal 'B' of transistor T1.

16. Remove the patch cord between socket '**E**' and '**F'** and connect a DMM through probes between the sockets '**E**' and '**F'**

17. Now set the digital multimeter's dial to DC current mode to measure the output DC Current, I_{out} between the sockets 'E' and '**F'** refer to figure).

18. Switch **on** the power supply.

19. Note down the value of output current $\mathbf{I_{out}}$ displayed on the DMM's display.

20. Ratio of output current to input current gives the overall of Darlington pair.

Calculate the ratio of output current to input current by following formula

$$\mathbf{\beta = I_{out} / I_i}$$

21. Individual of transistors can be calculated by considering the transistors having identical and using the formula

$$\mathbf{\beta = \beta_1 x\ \beta_2}$$

$$\mathbf{\beta_1 = \beta_2 = '\beta}$$

PROCEDURE FOR VOLTAGE GAIN:

1. Connect the Sockets '1' and '2' of **Sine Wave Generator** section to CRO channel CH1 through CRO probes

2. Switch **on** the power supply.

3. Using the **'Frequency control** ' and '**Amplitude control '** knobs of the **Sine Wave Generator** section, set the input signal at 1Vp-p, 1 KHz sine wave signal and observe the same on CRO channel CH1.
4. Switch **off** the power supply. Remove the CRO probes.
5. Connect a patch cord across sockets **'+12V '** of DC power supply and **'+12V '** of Emitter follower amplifier section.
6. Connect a patch cord between points '$\mathbf{V_{in}}$' and '1' and another patch cord between sockets '**G**1' and '2' in Emitter follower amplifier section.
7. Connect a patch cord between sockets '**B'** and 'D'.
8. Connect another patch cord between sockets '**E'** and 'F'.
9. Connect the Sockets '$\mathbf{V_{in}}$' and '**G**1'.
10. Connect the Sockets '$\mathbf{V_{out}}$' and '**G**2'.
11. Switch **on** the power supply.
12. Observe simultaneously the input waveform between points '$\mathbf{V_{in}}$**'** & '**G1'**display and measure the amplitude of input waveform. It is $\mathbf{V_{in}}$**.**
13. Also observe the output waveform between points '$\mathbf{V_{out}}$' and '**G2'** on CRO display and measure the amplitude of the output waveform. It is $\mathbf{V_{out}}$.
14. Calculate the voltage gain (it will be approximately equal to unity).

$$\mathbf{A_v = V_{out} / V_{in}}$$

CALCULATION:

CURRENT GAIN , INPUT IMPEDANCE :

$$I_i = (V_{in}\text{'} - V_{in}) / Rs$$

$$Z_{in} = V_{in} / I_i$$

$$\beta = I_{out} / I_i$$

$$\beta = \beta_1 \times \beta_2$$

VOLTAGE GAIN:

Voltage Gain, $Av = V_{out} / V_{in}$

Where, Vin = Input Voltage, Vout = Output Voltage

RESULT:

Current Gain of Darlington Pair, β =……

Individual β of transistor = β'=.....

Input impedance of emitter follower =……Ω

Voltage gain of Darlington pair =……..V

Input Current

Input Voltage, Vin = 4.40 V

Iin = [Vin1 - Vin] / Rs

Iin = [5 - 4.40] / 100 x 10^{3}

Iin = 6 µ A

Input Impedance

Zin = Vin/ Ii

Zin = 4.40 / 6 x 10^{-6}

Zin = 733 K

Output Current

Iout = 35.4 mA

Current Gain of Darlington Pair

β= Iout / Iin

β= 35.4 mA / 6 µA

β= 5900

Individual of transistor

β1 = β2 = β√= 76.8

Input Voltage

Vin = 1 Vpp

Output Voltage

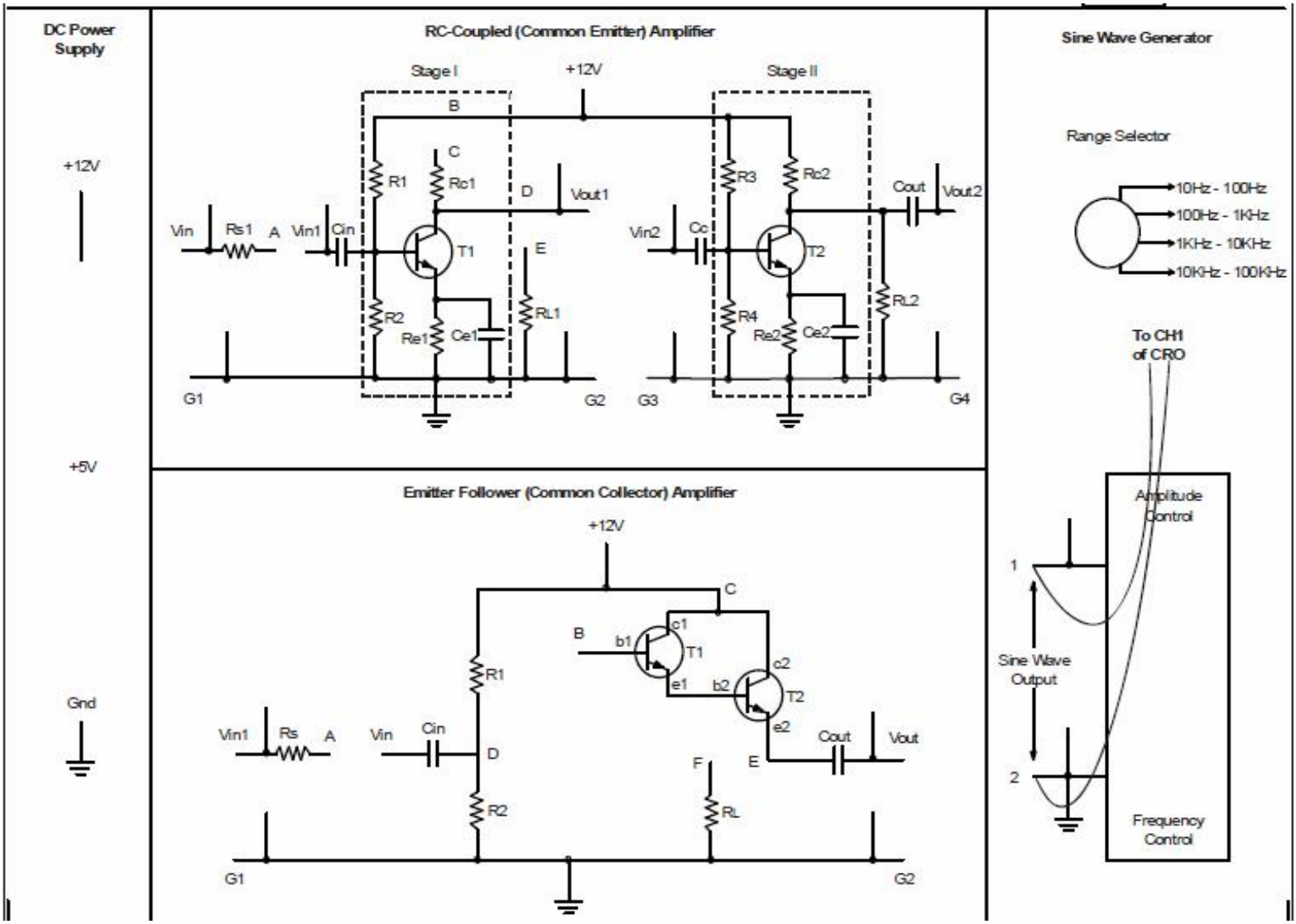
Vout == 1 Vpp

Voltage gain of Darlington pair

Av = Vout / Vin

Av = 1 Vpp / 1Vpp

Av = 1



Emitter Follower Amplifier using Darlington Pair

EXPERIMENT NO-7

AIM:- Power Amplifier: - Push Pull amplifier in class B mode of operation-measurement of gain.

APPARATUS:-

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	multimeter		1	
4.	CRO		1	

C.R.O , Power supply , Function generator, Bred-board & connection wires.

THEORY:-

A circuit arrangement of a Push Pull amplifier uses two transistors as shown in fig. This circuit ma work in class B or class A operation Class A amplifier has faithful amplification but they suffer from poor efficiency (about 35%). Therefore class B amplifiers which have higher efficiency are used at the O/P stage in push – pull arrangement. Because of circuit connection, it generates a very low distortion. In the circuit the excitation is introduced through a center tapped transformer. Thus, when the signal on transistor T_1 is positive, the signal on T_2 is negative by an equal amount. Any other circuit that provides equal voltages which differ in phases by 180° may be used in placed of the center tapped transformer. The collector terminal of the two transistors is connected to the supply V_{CC} through the primary of the transformer. The load resistance is connected across the secondary of the output transformer. Maximum Power is delivered here resistance R_1, R_2 and R_E from the biasing network. Almost all audio power amplifiers used in transistor radio receiver, tape record players ect. make use of this arrangement because these systems are usually operated by batteries or cells where efficiency is prime important. Even harmonics are reduced in O/P of this amplifier.

PROCEDURE:-

(1) Connect the circuit on bread-board as per the circuit diagram.

(2) Provide dc supply of +12V to the circuit.

(3) Feed ac signal of 1 kHz, 10mv at the I/P.

(4) Observe the O/P on C.R.O which will be an amplified one & calculate the gain of the signal.

OBSERVATIONS:-

S.NO	I/P FREQ. (fi)	I/P VOLTAGE (Vi)	O/P VOLTAGE (Vo)	GAIN

RESULT:- Thus we have studied class AB/B push –pull amplifier.

PRECATIONS:-

(1) Connection should be right & tight.

(2) Reading should be taken carefully.

(3) Supply should be switched – off after use.

EXPERIMENT NO-8

AIM:- Difference Amplifier:- Implementation of transistor differential amplifier.Non ideal characteristics of differential amplifier.

APPARATUS REQUIRED:

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	Multimeter		1	
4.	CRO		1	

CRO, Power Supply, resistance, bread-board, capacitor, connecting wires.

THEORY:

DIFFERENTIAL AMPLIFIER

A differential amplifier is most widely used circuit building block in analog integrated circuit. For instance, input stage of every op-amp amplifier is a differential amplifier. BJT differential amplifier is the basis of a very high speed logic circuit family called emitter-coupled logic (ECL). The differential amplifier as the name suggests amplifies the difference between two input signal v_{in1} and v_{in2}. BJT differential pair configuration consists of two matched transistors Q_1 and Q_2, whose emitters are formed together and biased by a constant current source I. Latter is usually implemented by a transistor circuit.The two collectors may be connected to another transistor rather than to resistive loads. It is essential though that the collector circuits be such that Q_1 and Q_2 can never enter saturation.

Gain of differential amplifier

$$A_d = \frac{v_0}{v_d}$$

where $v_d = v_{in1} - v_{in2}$

Non Ideal Characteristics

1. **Finite Gain**: open loop gain is infinite in the ideal differential amplifier but finite in real operational amplifier. In cases where closed loop be very high ,the feedback gain will be very low, and the low feedback gain causes low loop gain; in these case, the differential amplifier will be cease to behave ideally.
2. **Finite Input Impedance:** The input impedance of the differential amplifier is defined as the impedance between its two input. It is not the impedance from each input to ground. In the typical high gain the negative feedback applications.
3. **Non – zero output Impedance:** Low output impedance is important for low resistance loads; the voltage drop across the output impedance of the amplifier will be significant. Hence, the output impedance of the amplifier reflects the maximum power that can be provided.
4. **Input Offset Voltage:** This voltage, which is what is required across the differential amplifier input terminal to drive the output voltage to zero, is related to the mismatches in input biased current5 in the perfect amplifier, there would be no input offset voltage.
5. **Common Mode Gain:** A perfect differential amplifier amplifies only the voltage difference between its two inputs completely rejected all voltage that are common to both. However the differential input stage of differential amplifier is never perfect, leading to the amplification of these identical voltages to some degree.

PROCEDURE

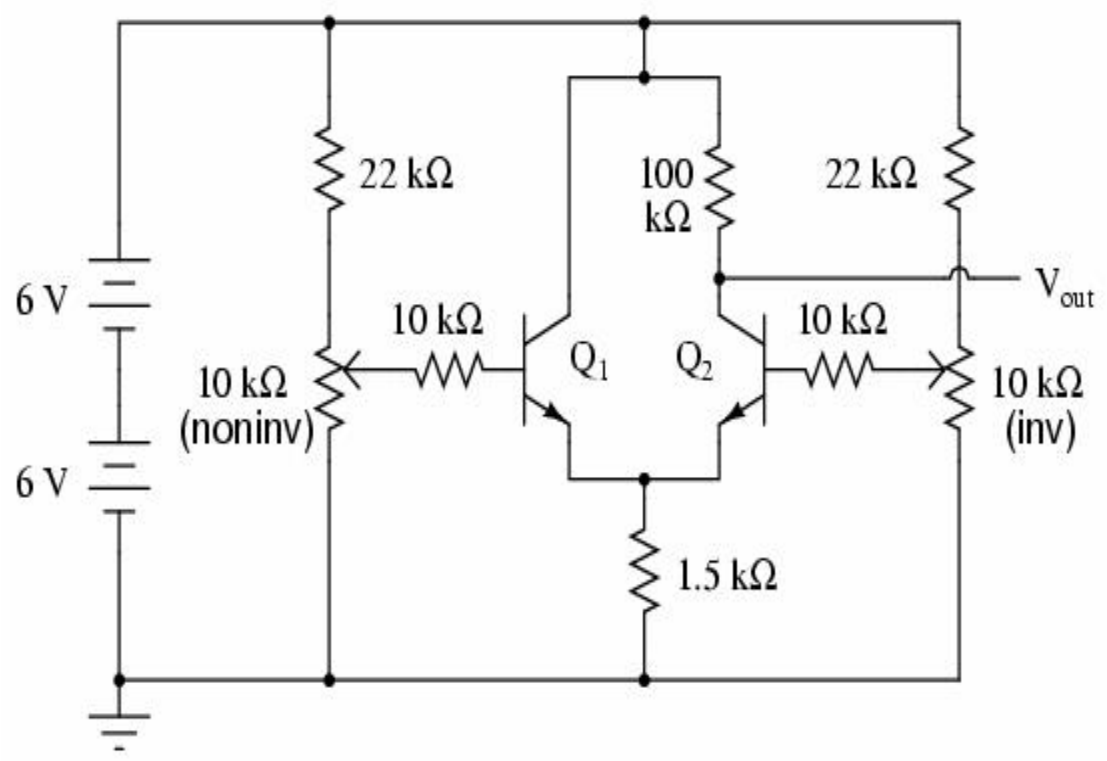
1. Connect the circuit as per diagram on the bread-board.
2. Connect 12V power supply.
3. Connect the v_{in1} and v_{in2} voltages to the circuit.
4. Measure the output voltage.

RESULT:

The gain of the differential amplifier is calculated as _____.

PRECAUTIONS:

1. All connection should be right & tight.
2. Reading should be taken carefully.
3. Power Supply should be switched OFF after use.



DIFFERENTIAL AMPLIFIER

EXPERIMENT NO – 9

AIM:- Oscillators:- Sinusoidal Oscillator – (a) Wein bridge Oscillator

(b) Phase shift Oscillator

APPARATUS:-

S no.	Particulars	Specification/Range	Quantity	Make/Model No.
1.	Trainer kit		1	
2.	Connecting wires			
3.	multimeter		1	
4.	CRO		1	

CRO ,Power supply , Bread–Board , IC 741, Resistor (3.3kΩ-2, 10kΩ), Capacitors (0.05Mf-2).

THEORY:- The **Wein-bridge Oscillator** is a standard circuit for generating low frequency in the rang of 10 HZ to 1MHZ . It is used all commercial audio generator. Wein-bridge is a ac bridge which balances only at particular frequency called null frequency. When the bridge is balanced the output of bridge is zero. For Oscillations to be sustained the phase shift to through the coupling network must be zero. It can be shown that this condition occurs at a frequency given by

$$F_O = 1/2\Pi RC$$

Here op-amp is used in non-inverting configuration and provides O^o phase shift. Since input impedance is large and out put impedance is small for the OP-AMP, there is no loading on the feed back network. When the above condition is satisfied we must have

$$\beta = 1/3$$

This means that amplifier must have a gain of at lest 3.

The **Phase Shift oscillator** produces positive feed back by using an inverting amplifier and adding another $180^0$of phase shift with the three high pass filter circuit. It produces this 180^ophase shift for only one frequency.

$$F_O = \frac{1}{2\Pi RC\sqrt{6}}$$

At which the feed back fraction is

$$\beta = 1/29$$

This means that amplifier must have a gain of at lest 29

PROCEDURE:-

(1) Connect the circuit as per the diagram. on the bread-board .

(2) Provide +/-12V Supply to the circuit.

(3) Observe the output sine wave on the CRO.

(4) Note the time period of this wave and calculate its frequency. Also calculate the gain.

OBSERVATION:-

1. Calculate value of frequency of w.b. ocs. using the formula Wein-bridge

$$F_o = \frac{1}{2\pi RC}$$

2.Calculate value of frequency of w.b. ocs. using the formula Wein-bridge

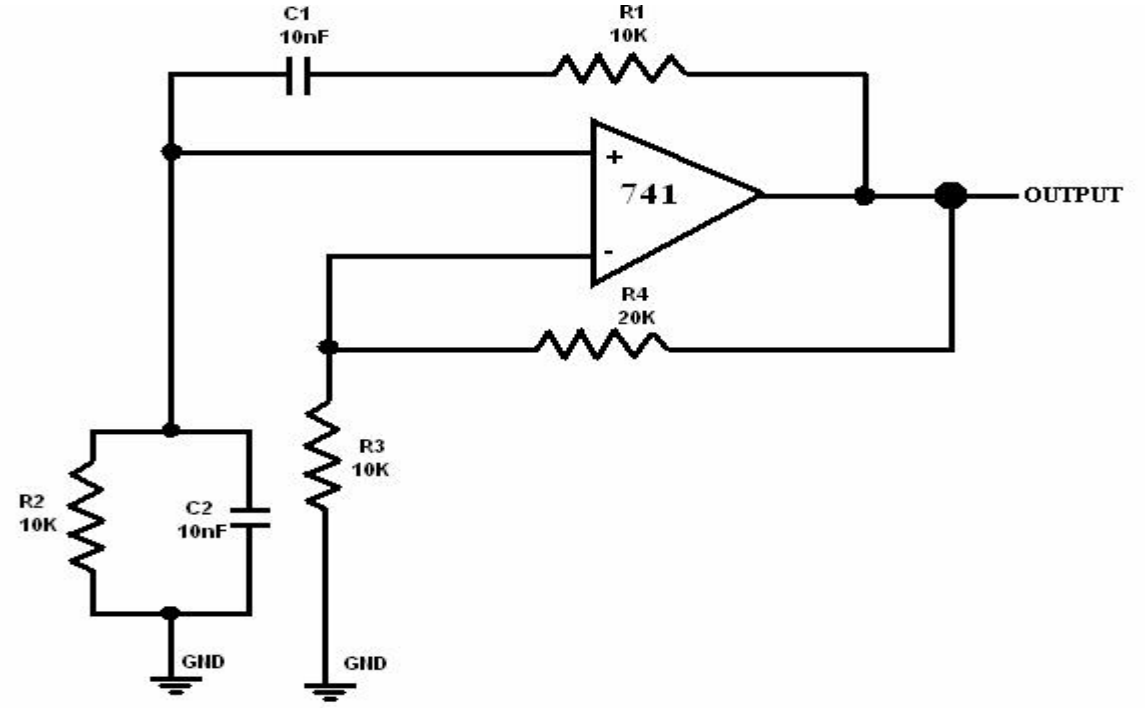
$$F_o = \frac{1}{2II\ RC\ \sqrt{6}}$$

3 . Practical Value of frequency as observed on CRO.

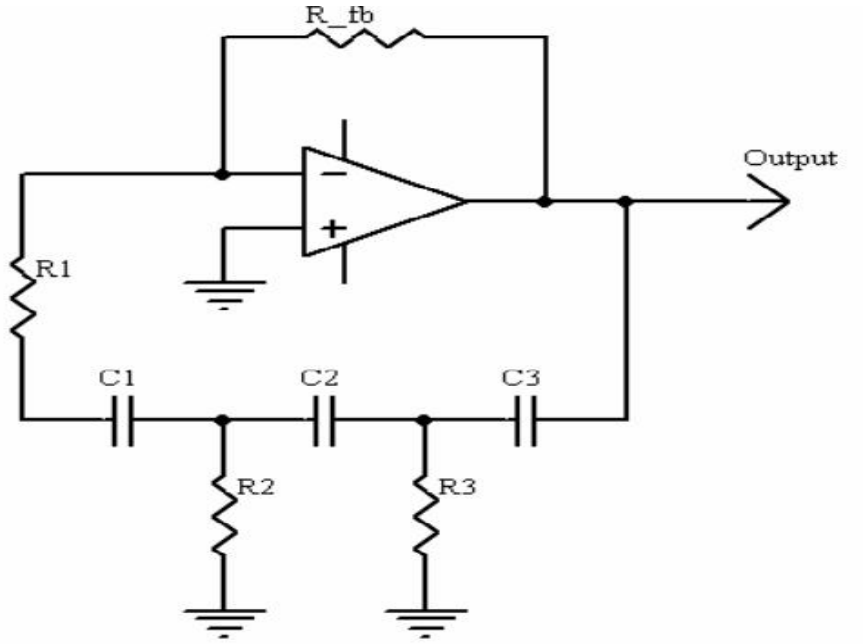
RESULT:- 1. Thus we have measured the frequency and gain for sine wave generated by Wein-bridge oscillator.

PRECAUTION:-

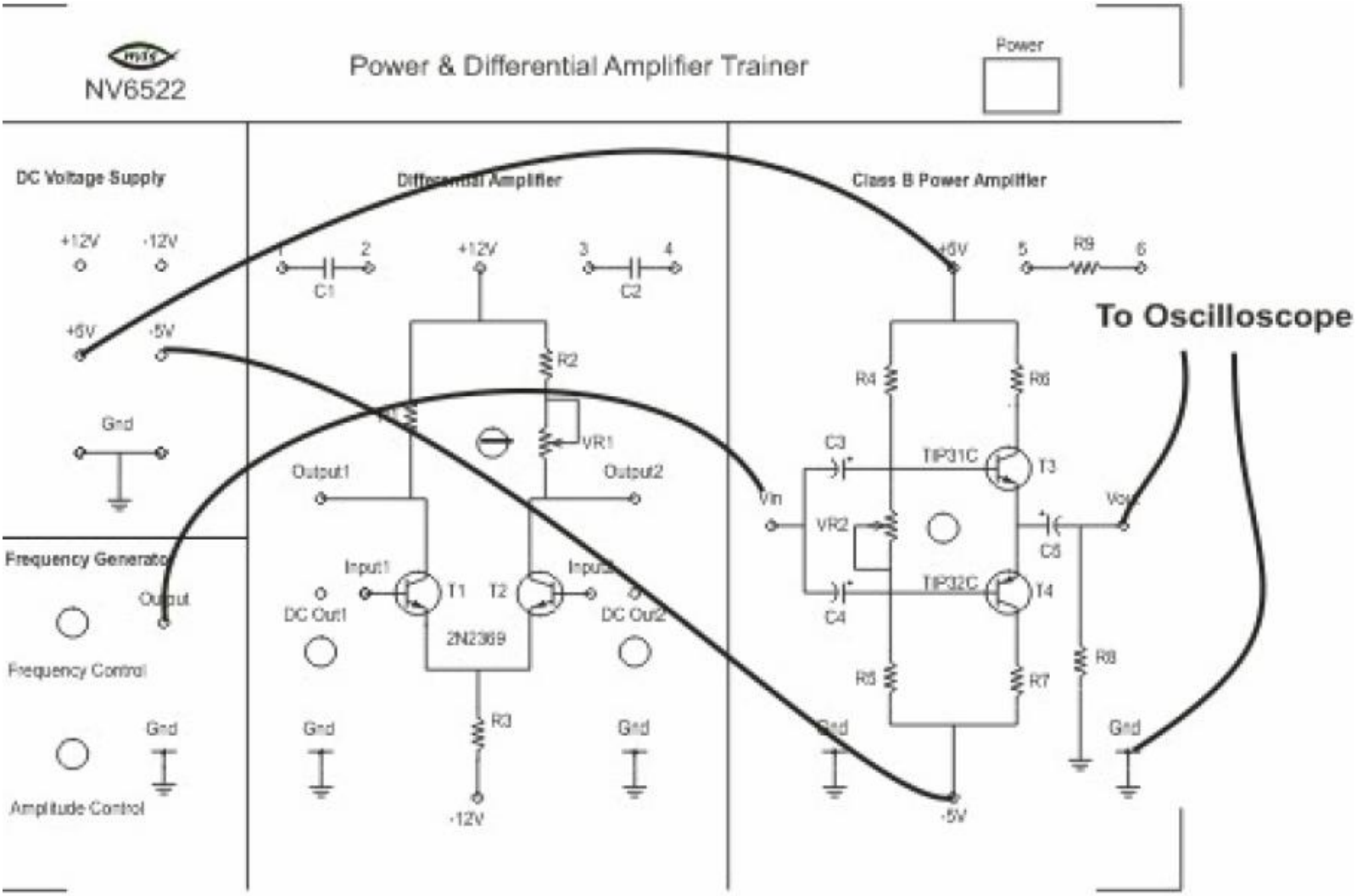
1. All connections should be right and tight.
2. Readings should be taken carefully.
3. Power supply should be switched off after use.



Circuit diagram for wein bridge oscillator



Circuit diagram for phase shift oscillator



EXPERIMENT NO – 10

OBJECTIVE:- To simulate of common emitter amplifier using PSpice.

SOFTWARE REQUIRED:- CADENCE _16.3

THEORY:- A transistor is a three-terminal active device. The three terminals are emitter, base and collector. For normal operation emitter- base junction is FB & collector base junction is RB. The I/P characteristic is a plot between I_E & V_{EB} keeping voltage V_{CB} constant. This characteristic curves is very similar to that of a FB diode. The *I/P* characteristic curves are plotted between Ic & V_{CB}, keeping IE constant. These curves are almost horizontal. The collector current Ic is less than, but almost equal to the emitter current. The current divide into Ic & l_B. That is
$I_E = Ic + I_B$

COMMON-EMITTER CONFIGURATION (CE)

The common-emitter configuration (ce) is the most frequently used configuration in practical amplifier circuits, since it provides good voltage, current, and power gain. The input to the CE is applied to the base-emitter circuit and the output is taken from the collector-emitter circuit, making the emitter the element "common" to both input and output. The CE is set apart from the other configurations, because it is the only configuration that provides a phase reversal between input and output signals.

Input characteristics: Same as in the case of common-base configuration, the EB junction of the common-emitter configuration can also be considered as a forward biased diode, the current-voltage characteristics is similar to that of a diode:

$$I_B = I_O (e^{VBE/VT} - 1)$$

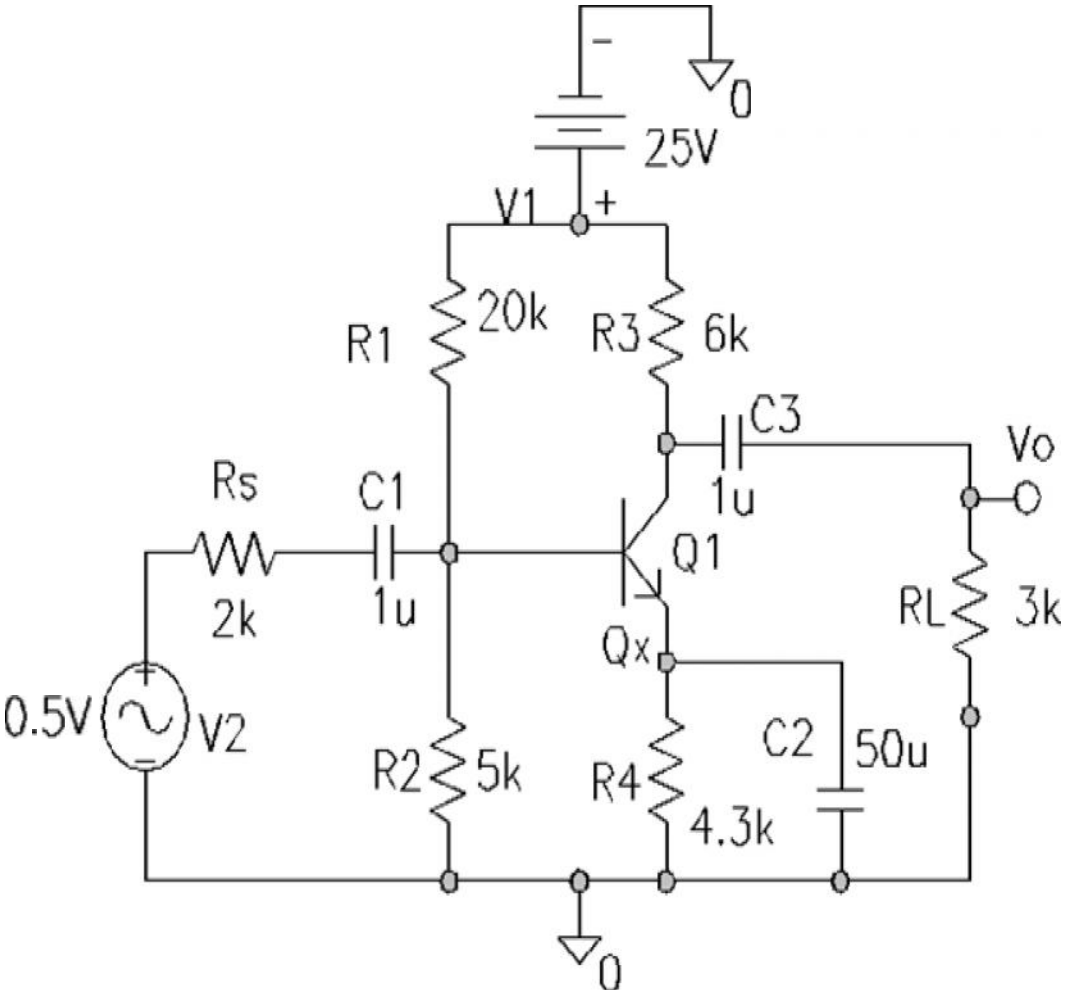
The collector-emitter voltage V_{CB} has little effect on I_B.

Output characteristics: The CB junction is reverse biased, the current

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

depends on the current I_B. When, $\boldsymbol{I_B = 0}$ & IC=$\boldsymbol{I_{CE0}}$ the current caused by the minority carriers crossing the P-N junctions. When I_B is increased, I_C is correspondingly increased by β fold (e.g. β=50,).

Circuit diagram



A Common-Emitter Amplifier

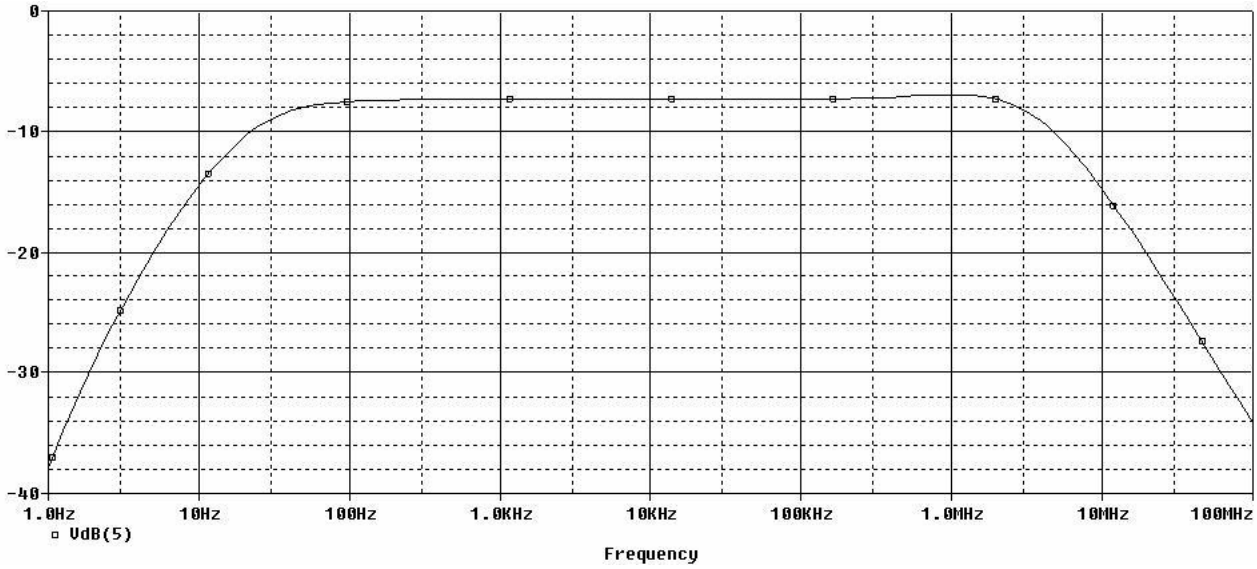
Figure shows a BJT common-emitter amplifier. The following `PSpice` script can be used to simulate the amplifier.

Program

```
Common Emitter Amplifier
* 25 July 1995--for PSpice6.3
V1 1 0 DC 25V
R1 1 2 20k
R2 2 0 5k
R3 1 3 6k
R4 4 0 4.3k
RL 5 0 3k
Rs 7 6 2k
C1 6 2 1u
```

C2 4 0 50u
C3 3 5 1u
Q2 3 2 4 Qx
.MODEL Qx NPN(BF=200)
VIN 7 0 DC 0 AC 0.5V
*analysis statements
.OP
.ac dec 10 10 10k
.probe
.END

RESULT:



PRECAUTIONS:

1. All the steps should be followed and circuit diagram should be correct.
2. Observe the result carefully.
3. System should be switched off after use.

PRE EXPERIMENT QUESTIONS:

Q. PSPICE stand for_____.

A. PSPICE stands for Personal Computer Simulation Program with Integrated Circuit.

Q. Name the different type of analysis used in PSPICE.
A. Transient analysis
Frequency response
AC analysis