DRONACHARYA
Group of Institutions

ANALOG CIRCUIT LAB

LABORATORY MANUAL

B.Tech. Semester -IV

Subject Code: KEC-452

Session: 2022-23, Even Semester

Name:	
Roll. No.:	
Group/Branch:	

DRONACHARYA GROUP OF INSTITUTIONS
DEPARTMENT OF ECZ
#27 KNOWLEDGE PARK 3

GREATER NOIDA

AFFILATED TO Dr. ABDUL KALAM TECHNICAL UNIVERSITY, LUCKNOW

Table of Contents

Vision and Mission of the Institute

Vision:

“Dronacharya Group of Institutions, Greater Noida aims to become an Institution of excellence in imparting quality Outcome Based Education that empowers the young generation with Knowledge, Skills, Research, Aptitude and Ethical values to solve Contemporary Challenging Problems”

Mission:

M1: To prepare students for full and ethical participation in a diverse society and encourage lifelong learning by following the principle of ‘Shiksha evam Sahayata’ i.e. Education and Help.

M2: To impart high-quality education, knowledge and technology through rigorous academic programs, cutting-edge research, and industry collaborations, with a focus on producing engineers and managers who are socially responsible, globally aware, and equipped to address complex challenges.

M3: Educate students in the best practices of the field as well as integrate the latest research into the academics.

M4: Provide quality learning experiences through effective classroom practices, innovative teaching practices, and opportunities for meaningful interactions between students and faculty.

M5: To devise and implement programmes of education in technology and management that are relevant to the changing needs of society, in terms of breadth of diversity and depth of specialization.

Vision and Mission of the Department

Vision:

V1: To be recognized as a department of excellence to produce competent and ethical students with a worldwide competency and shape them for industry, research, entrepreneurship and higher academic goals.

V2: The department's goal is to help students find, innovate, create, and produce environmentally friendly and socially responsible technology that fulfils the increasing demands of industry.

Mission:

M1: To impart to students technical and ethical knowledge to help them design, implement and control efficient systems and also comprehend the industry's expanding issues.

M2: Make every endeavor to engage with academic groups and industry to provide the framework for collaborative research.

Programme Educational Objectives (PEOs)

PEO 1. Engineers will practice the profession of engineering using a systems perspective and analyze, design, develop, optimize & implement engineering solutions and work productively as engineers, including supportive and leadership roles on multidisciplinary teams.

PEO 2. Continue their education in leading graduate programs in engineering & interdisciplinary areas to emerge as researchers, experts, educators & entrepreneurs and recognize the need for, and an ability to engage in continuing professional development and life-long learning.

PEO 3. Engineers, guided by the principles of sustainable development and global interconnectedness, will understand how engineering projects affect society and the environment.

PEO 4. Promote Design, Research, and implementation of products and services in the field of Engineering through Strong Communication and Entrepreneurial Skills.

PEO 5. Re-learn and innovate in ever-changing global economic and technological environments of the 21st century.

Programme Outcomes (POs)

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

ECZ

PSO1: Develop applications in the areas of Electronics and Computer Engineering based on the knowledge of Operating Systems, Signal processing, Computer Networks, Embedded Systems, Data analysis and algorithms.

PSO2: Ability to design, analyse, integrate and synthesize different novel systems to be capable for lifelong learning and advanced industrial research.

PSO3: Be proficient enough to make use of the technical concepts, suitable methods and algorithms for research as well as for the social needs.

University Syllabus

1. Characteristic of BJT: Study of BJT in various configurations (such as CE/CS, CB/CG,CC/CD).
2. BJT in CE configuration: Graphical measurement of h-parameters from input and output characteristics, measurement of Av, AI, Ro and Ri of CE amplifier with potential divider biasing.
3. Study of Multi-stage amplifiers: Frequency response of single stage and multistage amplifiers.
4. Feedback topologies: Study of voltage series, current series, voltage shunt, current shunt, effect of feedback on gain, bandwidth etc.
5. Measurement of Op-Amp parameters: Common mode gain, differential mode gain, CMRR, slew rate.
6. Applications of Op-Amp: Op-Amp as summing amplifier, difference amplifier, integrator and differentiator.
7. Field effect transistors: Single stage common source FET amplifier –plot of gain in dB vs frequency, measurement of bandwidth, input impedance, maximum signal handling capacity (MSHC) of an amplifier.
8. Oscillators: Study of sinusoidal oscillators- RC oscillators (phase shift, Wien bridge etc.).
9. Study of LC oscillators (Hartley, Colpitt, Clapp etc.)
10. Study of non-sinusoidal oscillators.
11. Simulation of amplifier circuits studied in the lab using any available simulation software and measurement of bandwidth and other parameters with the help of simulation software.
12. ADC/DAC: Design and study of Analog to Digital Converter.
13. Design and study of Digital to Analog Converter.

Course Outcomes (COs)

Upon successful completion of the course, the students will be able to:

CO1	Understand the characteristics of transistors.
CO2	Design and analyze various configurations of amplifier circuits.
CO3	Design sinusoidal and non-sinusoidal oscillators.
CO4	Understand the functioning of OP-AMP and design OP-AMP based circuits.
CO5	Design ADC and DAC.

CO-PO Mapping

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3			3						1		
CO2	2	3	2			2		2		2		2
CO3			3		3			1				1
CO4		2		3						2		2
CO5					3	3		2				
Course Correlation mapping	**1**	**1**	**1**	**1.2**	**1**	**1**		**1**	**1**	**1**		**1**

Correlation Levels: High-3, Medium-2, Low-1

CO-PSO Mapping

	PSO1	**PSO2**	**PSO3**
CO1	3		
CO2		3	2
CO3	2		3
CO4		3	
CO5		2	3
	1	1.6	1.6

Course Overview

In this lab students will study about the BJT and its various configurations (such as CE/CS, CB/CG, CC/CD), Graphical measurement of h-parameters from input and output characteristics, measurement of Av, AI, Ro and Ri of CE amplifier with potential divider biasing. Study of Multi-stage amplifiers: Frequency response of single stage and multistage amplifiers. Feedback topologies: Study of voltage series, current series, voltage shunt, current shunt, effect of feedback on gain, bandwidth etc. Measurement of Op-Amp parameters: Common mode gain, differential mode gain, CMRR, slew rate. Applications of Op-Amp: Op-Amp as summing amplifier, difference amplifier, integrator and differentiator. Field effect transistors: Single stage common source FET amplifier –plot of gain in dB vs frequency, measurement of bandwidth, input impedance, maximum signal handling capacity (MSHC) of an amplifier. Oscillators: Study of sinusoidal oscillators- RC oscillators (phase shift, Wien bridge etc.). Simulation of amplifier circuits studied in the lab using any available simulation software and measurement of bandwidth and other parameters with the help of simulation software. Design and study of Analog to Digital Converter and Digital to Analog Converter.

List of Experiments mapped with COs

S. No.	Name of the Experiment	Course Outcome
1	BJT characteristics (CE configuration)	**CO1**
2	BJT characteristics (CB configuration)	**CO1**
3	BJT characteristics (CC configuration)	**CO1**
4	FET characteristics	**CO2**
5	Frequency response of common source amplifier	**CO3**
6	Hartley oscillator	**CO4**
7	Colpitt's oscillator	**CO4**
8	Inverting amplifier	**CO1**
9	Non - inverting amplifier	**CO1**
10	Differentiator	**CO3**
11	Integrator	**CO3**

DOs and DON'Ts

DOs

1. Proper dress has to be maintained while entering in the Lab. (Boys Tuck in and shoes and girls should be neatly dressed)
2. Students should carry observation notes and record completed in all aspects.
3. Circuit diagram, tabular Colum and model graph should be in the observation before entering the lab.
4. Circuit and its theoretical result should be there in the observation before coming to the next lab.
5. Students must maintain silence while doing experiments.
6. Student should follow the lab procedure and get the components from the lab instructor.
7. After completing the experiment need to switch off the power supply, return the components to lab instructor safely and arrange the chairs properly.
8. The Practical Result should be noted down into their observations and result must be shown to the Lecturer In-Charge for verification.
9. Students must ensure that all switches are in the OFF position; main switch is shut down properly.

DON'Ts

1. Don't come late to the Lab.
2. Don't leave the Lab without making proper shut down of power supply and return safely to lab instructor.
3. Don't disrupt others while doing experiments.
4. Don't leave the Lab without verification by Lab instructor.
5. Don't leave the lab without the permission of the Lecturer In-Charge.

General Safety Precautions

Precautions (In case of Injury or Electric Shock)

1. To break the victim with live electric source, use an insulator such as fire wood or plastic to break the contact. Do not touch the victim with bare hands to avoid the risk of electrifying yourself.
2. Unplug the risk of faulty equipment. If main circuit breaker is accessible, turn the circuit off.
3. If the victim is unconscious, start resuscitation immediately, use your hands to press the chest in and out to continue breathing function. Use mouth-to-mouth resuscitation if necessary.
4. Immediately call medical emergency and security. Remember! Time is critical; be best.

Precautions (In case of Fire)

1. Turn the equipment off. If power switch is not immediately accessible, take plug off.
2. If fire continues, try to curb the fire, if possible, by using the fire extinguisher or by covering it with a heavy cloth if possible isolate the burning equipment from the other surrounding equipment.
3. Sound the fire alarm by activating the nearest alarm switch located in the hallway.
4. Call security and emergency department immediately:

Emergency : 201 (Reception)

Security : 231 (Gate No.1)

Guidelines to students for report preparation

All students are required to maintain a record of the experiments conducted by them. Guidelines for its preparation are as follows: -

1) All files must contain a title page followed by an index page. ***The files will not be signed by the faculty without an entry in the index page.***

2) Student's Name, Roll number and date of conduction of experiment must be written on all pages.

3) For each experiment, the record must contain the following

(i) Aim/Objective of the experiment
(ii) Pre-experiment work (as given by the faculty)
(iii) Lab assignment questions and their solutions
(iv) Test Cases (if applicable to the course)
(v) Results/ output

Note:

1. Students must bring their lab record along with them whenever they come for the lab.

2. Students must ensure that their lab record is regularly evaluated.

Lab Assessment Criteria

An estimated 10 lab classes are conducted in a semester for each lab course. These lab classes are assessed continuously. Each lab experiment is evaluated based on 5 assessment criteria as shown in following table. Assessed performance in each experiment is used to compute Course Outcomes attainment as well as internal marks in the lab course.

Grading Criteria	Exemplary (4)	Competent (3)	Needs Improvement (2)	Poor (1)
AC1: Designing experiments	The student chooses the problems to explore.	The student chooses the problems but does not set an appropriate goal for how to explore them.	The student fails to define the problem adequately.	The student does not identify the problem.
AC2: Collecting data through observation and/or experimentation	Develops a clear procedure for investigating the problem	Observations are completed with necessary theoretical calculations and proper identification of required components.	Observations are completed with necessary theoretical calculations but without proper understanding. Obtain the correct values for only a few components after calculations. Followed the given experimental procedures but obtained results with some errors.	Observations are incomplete. Lacks the appropriate knowledge of the lab procedures.
AC3: Interpreting data	Decides what data and observations are to be collected and verified	Can decide what data and observations are to be collected but lacks the knowledge to verify	Student decides what data to gather but not sufficient	Student has no knowledge of what data and observations are to be collected
AC4: Drawing conclusions	Interprets and analyses the data in order to propose viable conclusions and solutions	Incomplete analysis of data hence the quality of conclusions drawn is not up to the mark	Cannot analyse the data or observations for any kind of conclusions.	Lacks the required knowledge to propose viable conclusions and solutions
AC5: Lab record assessment	Well-organized and confident presentation of record & ability to correlate the theoretical concepts with the concerned lab results with appropriate reasons.	Presentation of record is acceptable	Presentation of record lacks clarity and organization	No efforts were exhibited

LAB EXPERIMENTS

1. BJT CHARACTERISTICS (CE Configuration)

AIM: To observe the characteristics of BJT while it is in CE configuration mode.

APPARATUS:

Regulated Power Supply (0-15V)

BJT

Resistors
Capacitors
Voltmeter
Multimeter

Breadboard

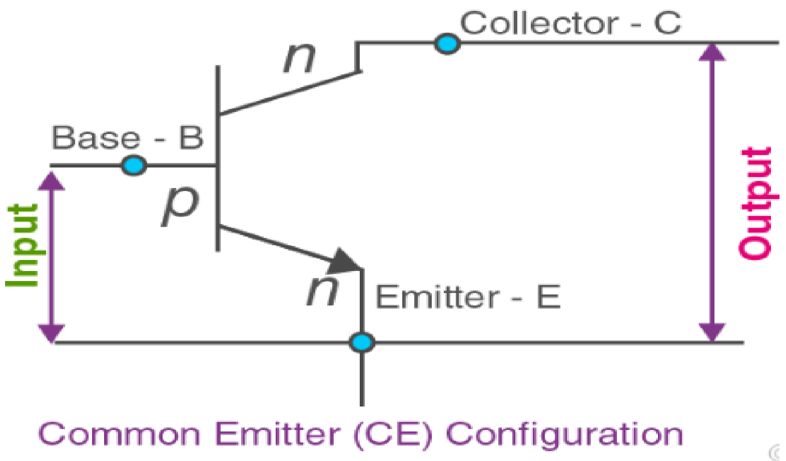
Connecting Wires

PROCEDURE:

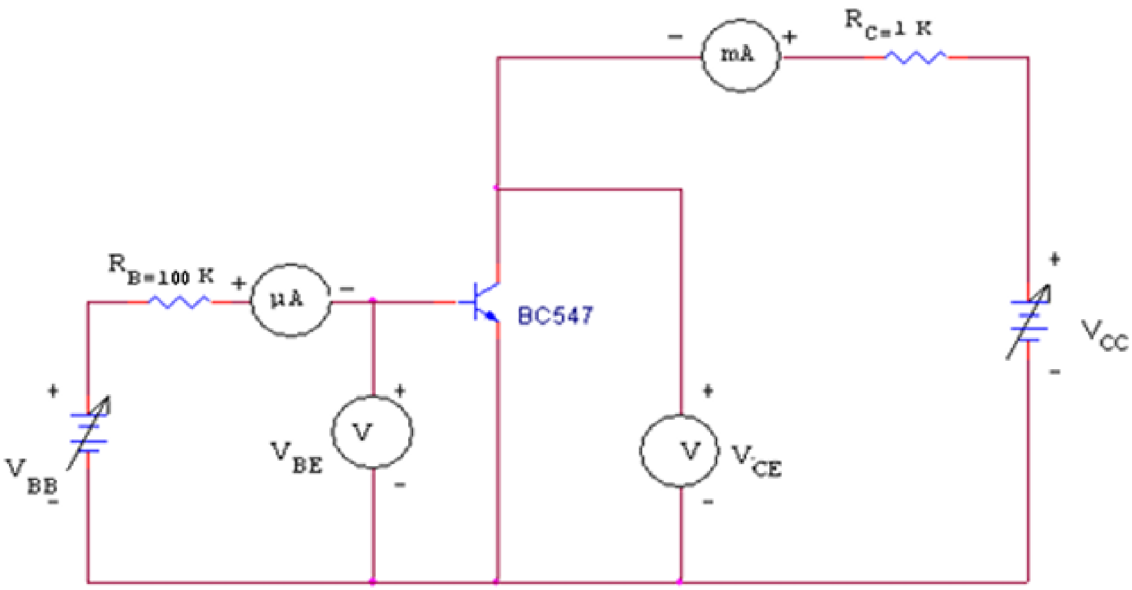
1. Connection is made as per circuit diagram.
2. To absorb the voltage.
3. To absorb the current.
3. Tabulate the readings.
4. To plot the graph.

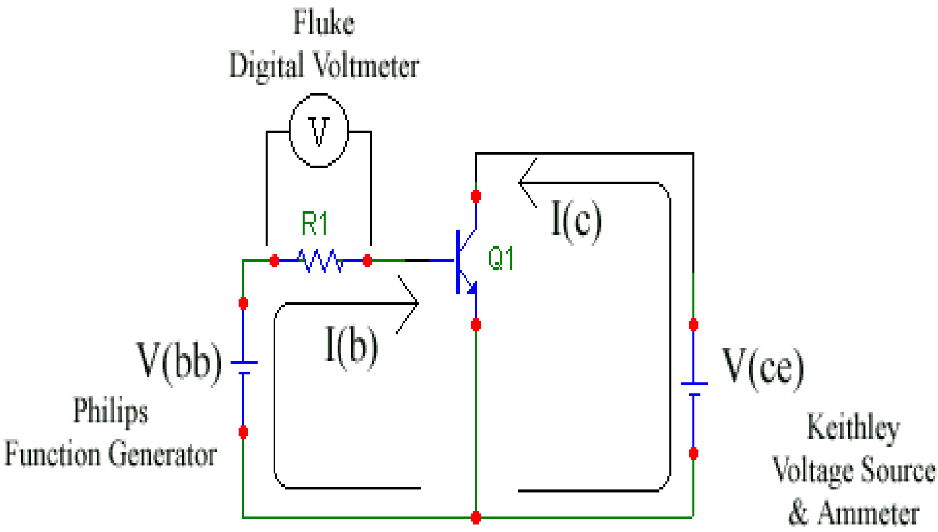
THEORY:

The configuration in which the emitter is connected between the collector and base is known as a common emitter configuration. The variation of emitter current (I_B) with Base-Emitter voltage(V_{BE}), keeping Collector Emitter voltage(V_{CE}) constant.



CIRCUIT DIAGRAM





Result: Thus studied the characteristics of BJT while it is in CE configuration mode.

Department of ECZ 2022-23

2. BJT CHARACTERISTICS (CB Configuration)

AIM: To observe the characteristics of BJT while it is in CB configuration mode.

APPARATUS:

Regulated Power Supply (0-15V)

BJT

Resistors
Capacoitors
Voltmeter
Multimeter

Breadboard

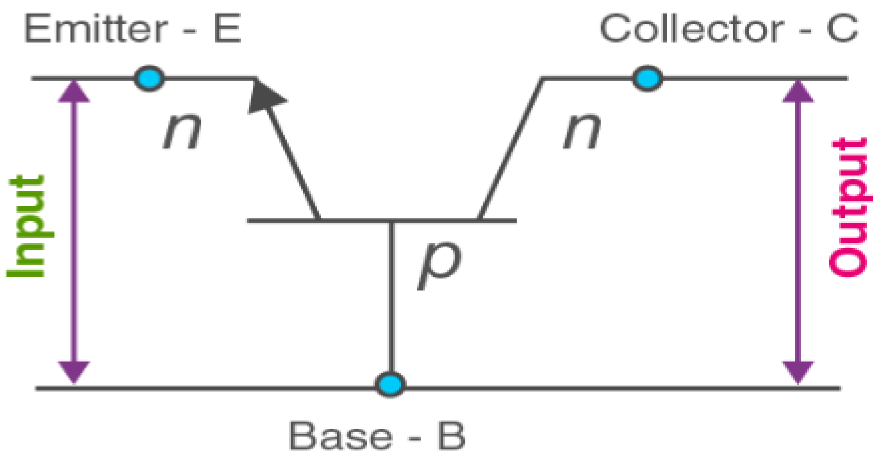
Connecting Wires

PROCEDURE:

1. Connection is made as per circuit diagram.
2. To absorb the voltage.
3. To absorb the current.
3. Tabulate the readings.
4. To plot the graph.

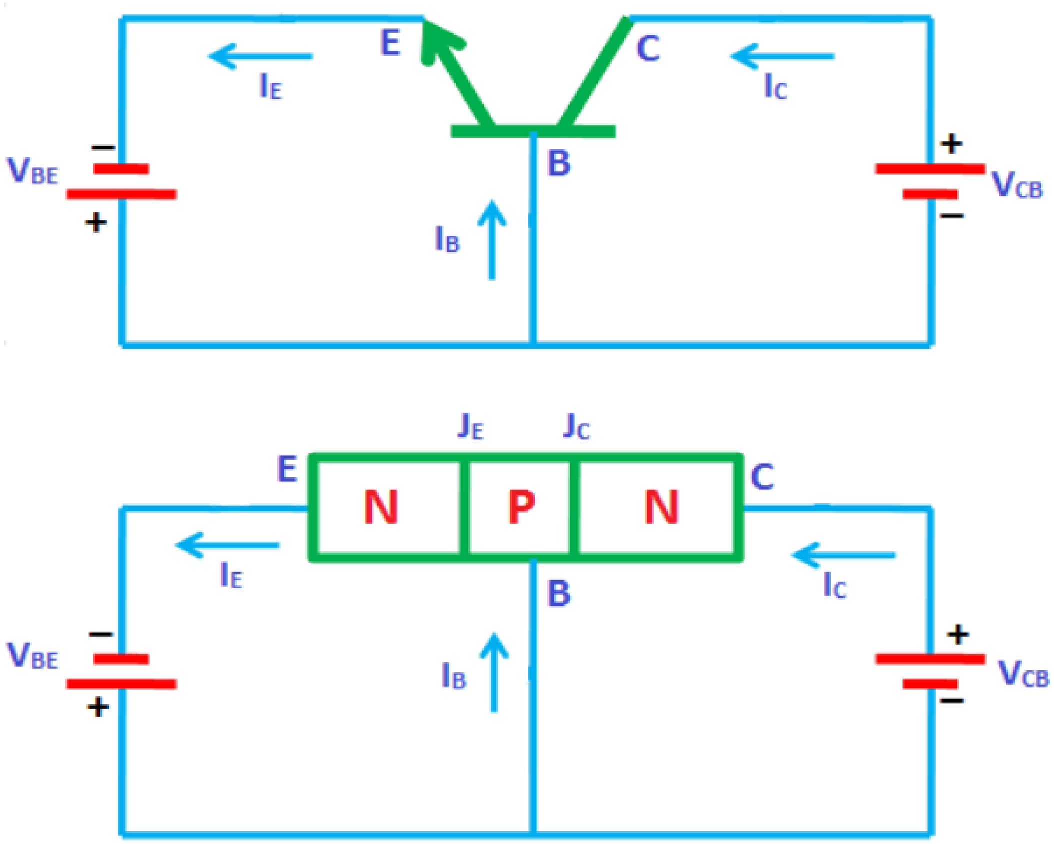
THEORY:

In CB Configuration, the base terminal of the transistor will be connected common between the output and the input terminals. The variation of emitter current (I_E) with Base-Emitter voltage (V_{BE}), keeping Collector Base voltage(V_{CB}) constant.



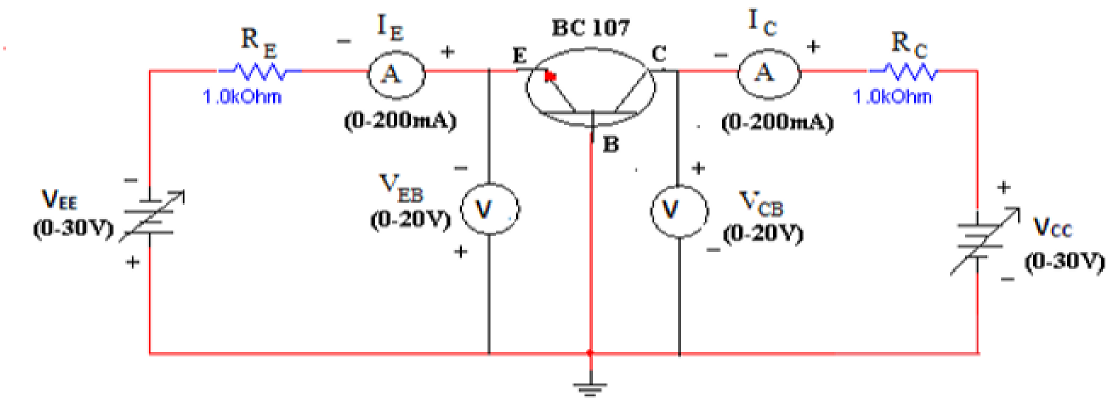
Common base (CB) Configuration

Department of ECZ 2022-23



Common base configuration

CIRCUIT DIAGRAM



Result: Thus studied the characteristics of BJT while it is in CB configuration mode.

Department of ECZ 2022-23

3. BJT CHARACTERISTICS (CC Configuration)

AIM: To observe the characteristics of BJT while it is in CC configuration mode.

APPARATUS:

Regulated Power Supply (0-15V)

BJT

Resistors
Capacoitors
Voltmeter
Multimeter

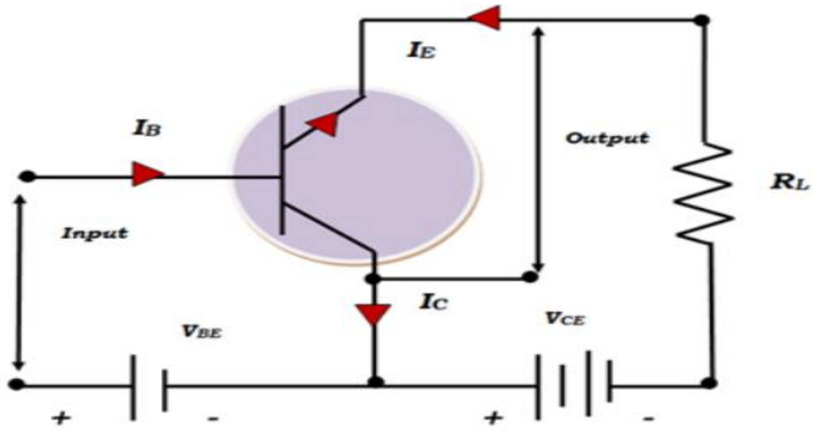
Breadboard

Connecting Wires

PROCEDURE:

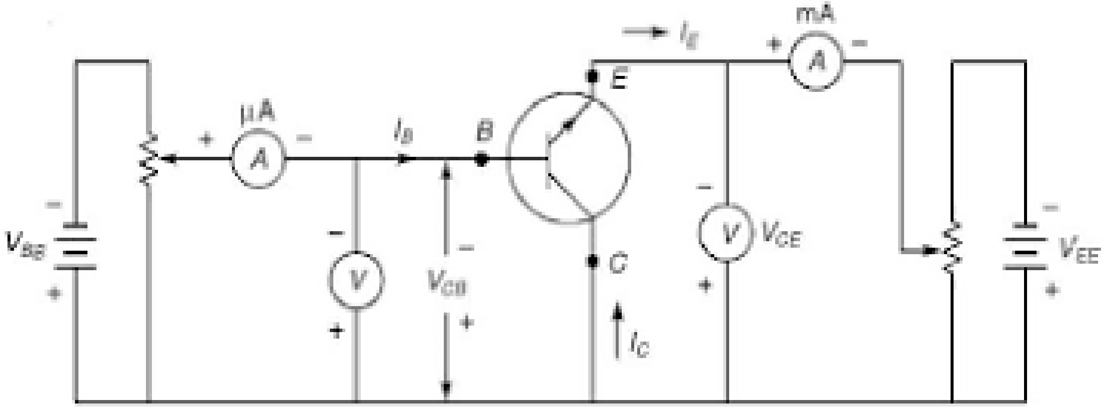
1. Connection is made as per circuit diagram.
2. To absorb the voltage.
3. To absorb the current.
3. Tabulate the readings.
4. To plot the graph.

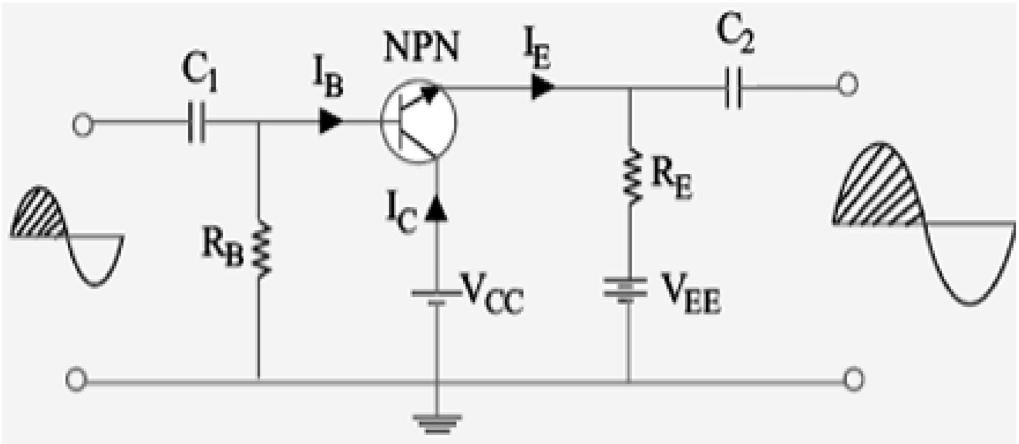
THEORY: The common collector configuration is also called emitter follower or voltage follower because the output emitter voltage always follows the base input voltage. For example the base emitter voltage is 0.7v and if the input is 5V then the output is 4.3V. Output voltage is always near the input voltage. This configuration is widely used as a buffer and it is also called as voltage buffer.



CIRCUIT DIAGRAM

Department of ECZ 2022-23





Result: Thus studied the characteristics of BJT while it is in CC configuration mode.

Department of ECZ 2022-23

4. FET CHARACTERISTICS

AIM: To draw the drain and transfer characteristics of a given FET.

APPARATUS:

JFET (BFW11)

Regulated Power Supply (0-15V)

Voltmeter (0-20V)

Ammeter (0-200mA)

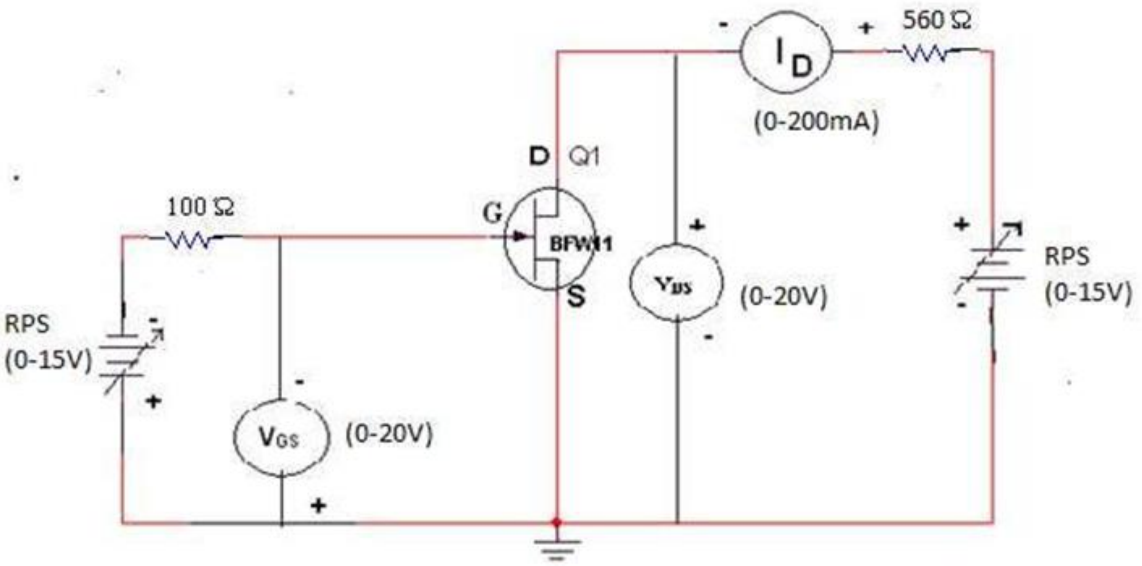
Breadboard,
Connecting wires

THEORY:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with V_{DS}. With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called "pinch of voltage". If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased. In amplifier application, the FET is always used in the region beyond the pinch-off.

$F_{DS} = I_{DSS} (1-V_{GS}/V_P)^2$

CIRCUIT DIAGRAM:



Department of ECZ 2022-23

PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep V_{GS} constant at 0V.
3. Vary the V_{DD} and observe the values of V_{DS} and I_D.
4. Repeat the above steps 2, 3 for different values of V_{GS} at 0.1V and 0.2V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep V_{DS} constant at 1V.
7. Vary V_{GG} and observe the values of V_{GS} and I_D.
8. Repeat steps 6 and 7 for different values of V_{DS} at 1.5 V and 2V.
9. The readings are tabulated.

OBSERVATIONS:

DRAIN CHARACTERISTICS:

S.NO	V_{GS}=0V		V_{GS}=-1V		V_{GS}=-2V	
	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

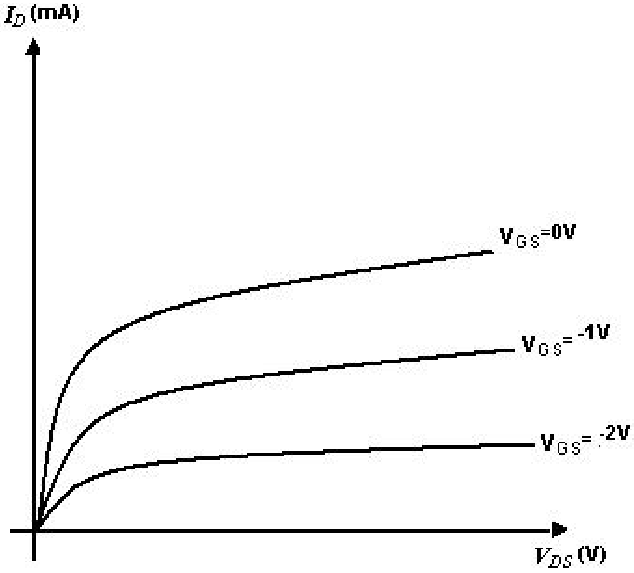
TRANSFER CHARACTERISTICS:

S.NO	V_{DS} =0.5V		V_{DS}=1V		V_{DS} =1.5V	
	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)

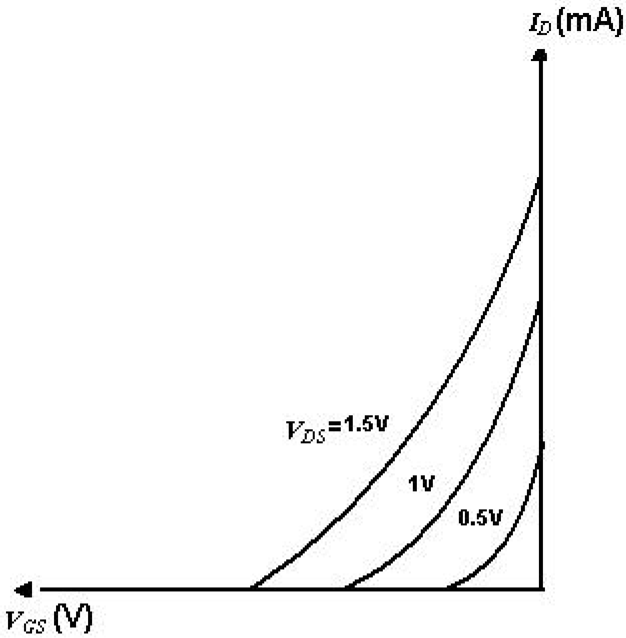
Department of ECZ 2022-23

MODEL GRAPH:

DRAIN CHARACTERISTICS:



TRANSFER CHARACTERISTICS:



RESULT: The drain and transfer characteristics of a FET are drawn.

5. FREQUENCY RESPONSE OF COMMON SOURCE AMPLIFIER

AIM: To find the frequency response and bandwidth of a given single stage FET amplifier.

APPARATUS:

JFET - BFW11

Resistors - 1 KΩ, 10 KΩ, 10 KΩ, 470 Ω

Capacitors - 1 μ F, 0.01 μ F, 47μ F/40V

Regulated Power Supply – (0-15V)

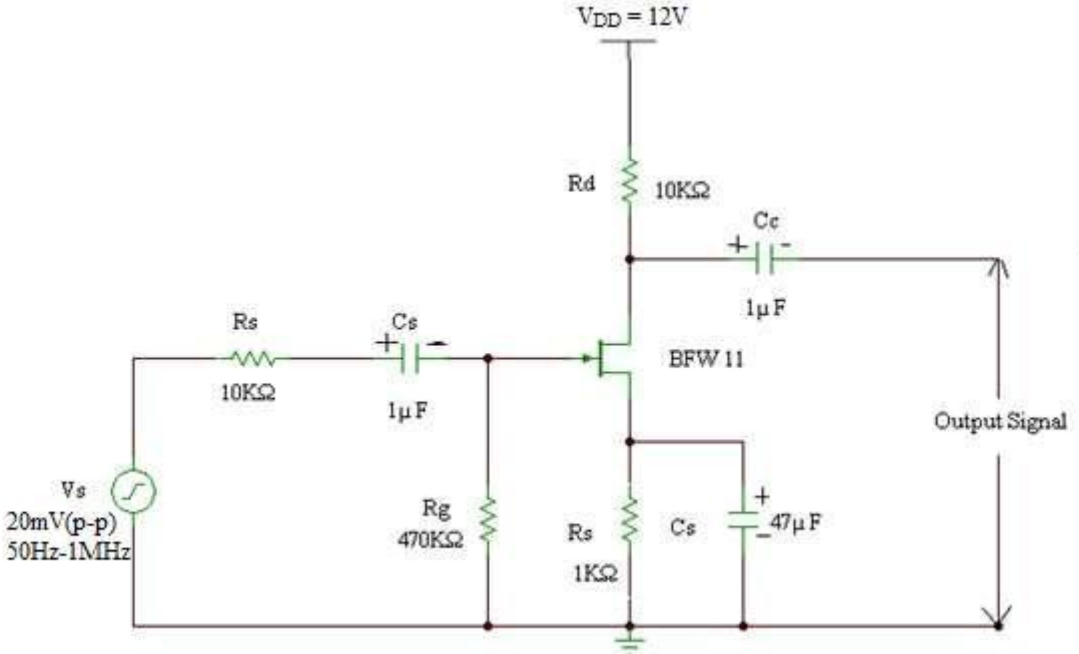
Signal Generator

CRO

THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide- semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle. The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification,
such as is required in large wireless communications and broadcast transmitters

CIRCUIT DIAGRAM:



PROCEDURE:

1. As per the design specifications, connect the circuit as shown.
2. Set the frequency of I/P signal at 5 KHz and increase the amplitude, till O/P gets distorted. The value of I/P signal is maximum signal handling capacity.
3. Set I/P signal at a constant value, less than the maximum signal handling capacity, vary frequency in the range 50Hz to 1MHz and find O/P voltage for each and every frequency.
4. Calculate voltage gain at each and every frequency.
5. Plot the frequency versus gain and determine f_H and f_L.
6. Calculate bandwidth f_H - f_L.
7. Procedure for measuring input impedance: Set the signal generator frequency at 2KHz

   and measure V_s and V_i. Then $I_i = V_s - V_i / R_S$. I/P impedance =

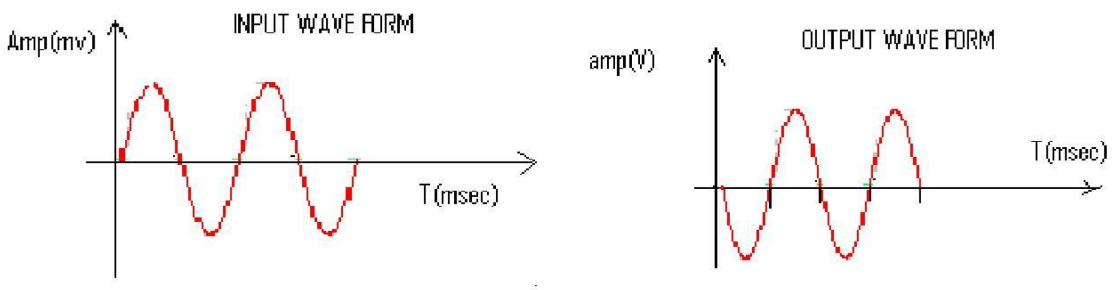
   V_i / I_i
8. Procedure for measuring O/P impedance: Open the O/P circuit and measure voltage (V open) across O/P using CRO. After connecting variable resistor at O/P terminals, vary the resistance to make the O/P (V open) become to half of its value. Then

   existing resistance is its O/P resistance.

OBSERVATIONS:

S. No	Frequency (Hz)	O/P voltage (V_0)	Gain (V_0/ V_I)	Gain in dB 20*$\log_{10}(V_0 / V_I)$

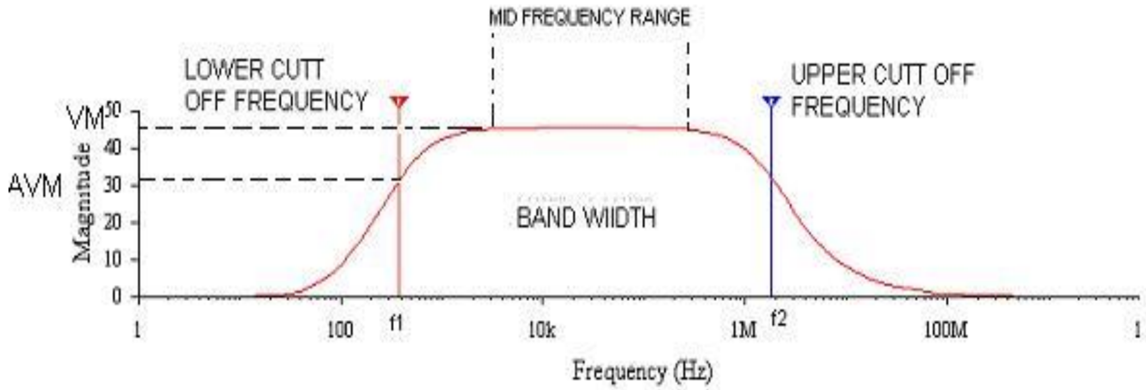
MODEL WAVEFORMS:



FREQUENCY PLOT:

A graph is plotted between f on X – axis and 20*$\log_{10}$ (V_0 / V_I) on Y-axis on a semi-log sheet. It will be as shown in figure.

$BW = f_H – f_L$



RESULT: The frequency response curve for a common source FET Amplifier is plotted and its bandwidth is obtained.

6. Hartley oscillator

AIM

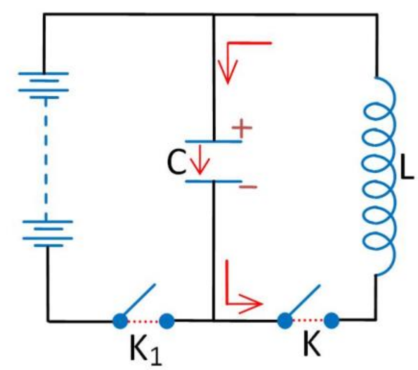
To design and construct a Hartley oscillator and to measure its output frequency.

COMPONENTS

Transistors, Bread board, resistors, capacitors, inductance coil, dc power supply, C.R.O, connection wires etc

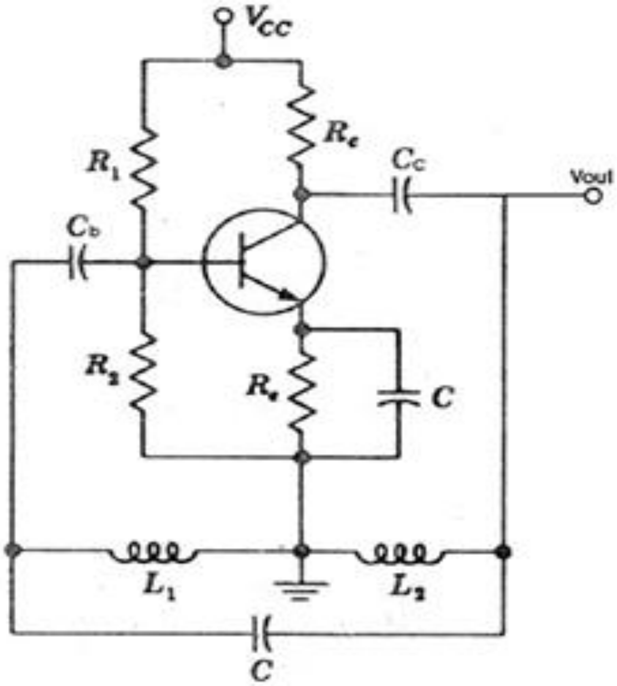
THEORY

A circuit which produces electrical oscillations of any desired frequency is known as an oscillatory circuit. A simple oscillatory circuit is one which contains a capacitor C and inductor L placed in parallel as shown.When the key K1 is closed, the capacitor C is charged with upper plate positive and lower plate negative. Now the key K1 is kept open. At this moment lower plate has an excess and upper plate a deficit of electrons. This gives rise to an electric field across the capacitor plates in the direction shown. When the key K is closed, the capacitor discharges itself through inductor and there is a flow of electrons as indicated by arrow head. The current flow sets up a magnetic field around the inductor coil. Due to inductive effect the current builds up slowly up to a maximum value which is attained when the capacitor is fully discharged. At that instant the electrostatic energy is zero but due to maximum current flow the magnetic field energy around the inductor coil is at maximum. As the capacitor is fully discharged the magnetic field starts decreasing. As the magnetic flux linked with circuit changes, an e.m.f is induced, which makes the current to flow. This current recharges the capacitor in opposite direction with its upper plate negative and lower plate positive. Finally the magnetic field fully collapses. At this stage the magnetic field energy is zero and electrostatic energy is again at maximum.

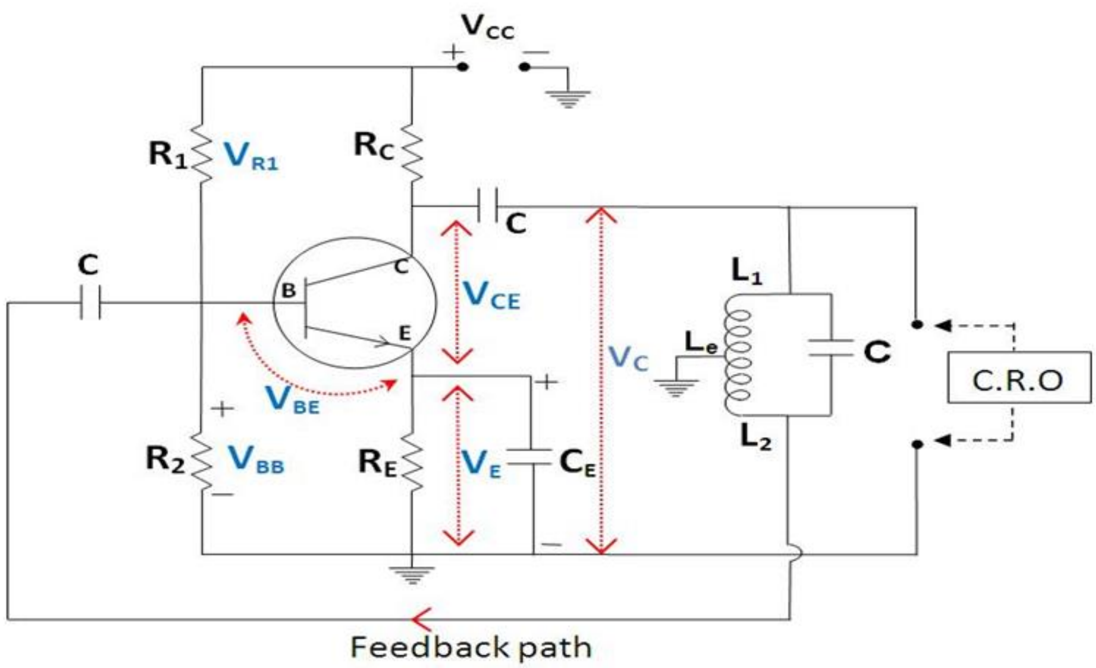


As soon as the magnetic field is zero, the capacitor which is fully recharged begins to discharge, due to which the current flows in opposite direction and a magnetic field is again set up around the inductor coil. The magnetic field energy becomes a maximum when electric field energy is zero. Hartley Oscillator is a device that generates oscillatory output (sinusoidal). It consists of an amplifier linked to an oscillatory circuit, also called LC circuit or tank circuit. The function of tank circuit is to tune a certain frequency. LC oscillators are designed to operate in the radio-frequency range. Its inductance will be in micro Henries. However they can also be designed to produce oscillations in the low audio-frequency range. But for the low-frequency operation, the inductors used will be very large in value, i.e of milli Henrie range and hence very large in physical size.

CIRCUIT DIAGRAM



Hartley Oscillator

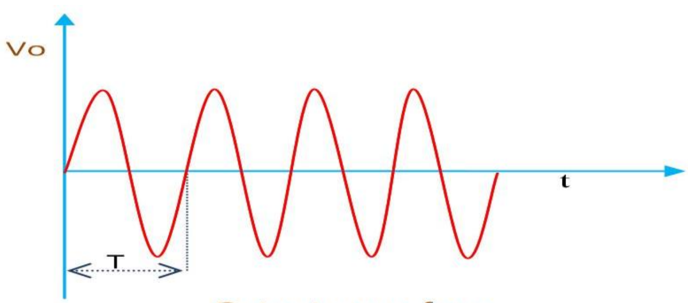


WORKING

When the supply is switched–on, a voltage V_1 is developed across L_1 and V_2 across L_2.V_1 is the oscillator output. There is a phase difference of 180^0 between the voltage of L_1 and L_2.The voltage across L_2 (V_2) is given as the feedback signal. Since the amplifier is in CE configuration, it produces a phase difference of 180^0.Therfore amplifier and the feedback network together produces a phase difference of 360^0.i.e, a positive feedback is achieved and circuit work as an oscillator. Once energy is supplied to the tank circuit, cycle begins. The capacitor stores energy in its electric field whenever there is a potential difference across its plates. As the current begins to flow out of the capacitor and into the inductor, a magnetic field builds up around the coil. Capacitor loses its energy and current will continue to flow in the inductor caused by the effect of the energy in the magnetic field. This current will start to send current back into the capacitor, in reverse direction. The cycle then repeats, over and over, at a period (frequency) that is determined by the values of the inductor, the capacitor.The frequency of oscillation is given by

$$f = \frac{1}{2\pi\sqrt{LC}}$$

This is our output wave form.



Output wave form

RESULT

Amplitude and frequency of sine wave from Hartley Oscillator =……V...Hz.

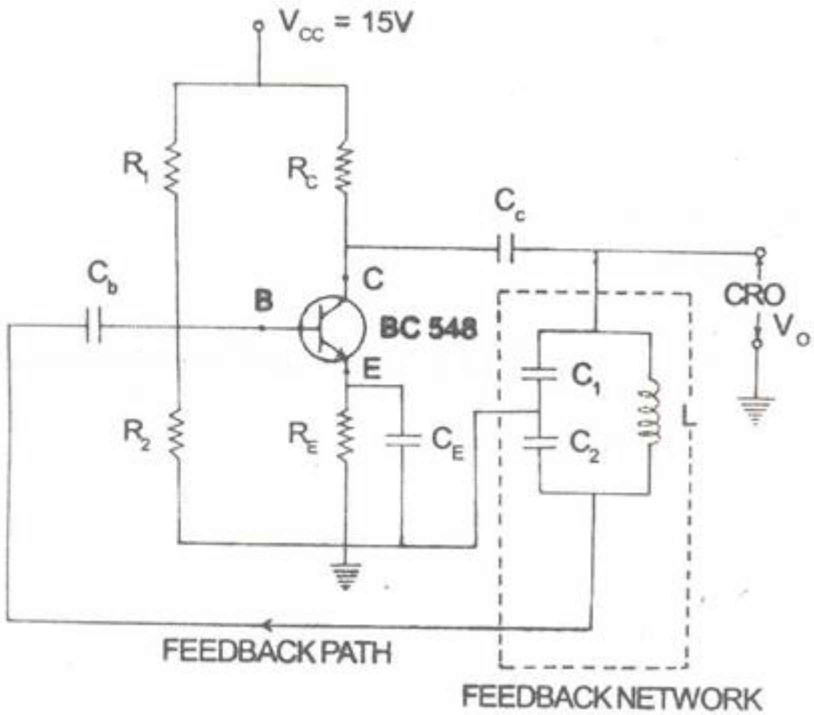
7. Colpitt's oscillator

Aim :- To construct Colpitt's oscillator using a transistor, to find out the frequency of oscillation and comparing it to that of theoretical frequency.

Apparatus :- n-p-n transistor, Carbon resistors (as shown in circuit), inductor, capacitors, dc power supply, CRO and connecting terminals.

Description :- The Colpitt's oscillator is designed for generation of high frequency sinusoidal oscillations (radio frequencies ranging from 10KHz to 100MHz). They are widely used in commercial signal generators up to 100MHz. Colpitt's oscillator is same as Hartley oscillator except for one difference. Instead of using a tapped inductance, Colpitt's oscillator uses a tapped capacitance. The circuit diagram of Colpitt's oscillator using BJT is shown in Fig. It consists of an R-C coupled amplifier using an n-p-n transistor in CE configuration. R1 and R2 are two resistors which form a voltage divider bias to the transistor. A resistor RE is connected in the circuit which stabilizes the circuit against temperature variations. A capacitor CE is connected in parallel with RE, acts as a bypass capacitor and provides a low reactive path to the amplified ac signal. The coupling capacitor CC blocks dc and provides an ac path from the collector to the tank circuit. The feedback network (tank circuit) consists of two capacitors C1 and C2 (in series) which placed across a common inductor L. The centre of the two capacitors is tapped (grounded). The feedback network (C1, C2 and L) determines the frequency of Page 2 of 3 oscillation of the oscillator. The two series capacitors C1, and C2 form the potential divider led for providing the feedback voltage. The voltage developed across the capacitor C2 provides regenerative feedback which is essential for sustained oscillations. When the collector supply voltage Vcc is switched on, collector current starts rising and charges the capacitors C1 and C2. When these capacitors are fully charged, they discharge through coil L setting up damped harmonic oscillations in the tank circuit. The oscillatory current in the tank circuit produces an a.c. voltages across C1, C2. The oscillations across C2 are applied to base-emitter junction of the transistor and appears in the amplified form in the collector circuit and overcomes the losses occurring in the tank circuit. The feedback voltage (across the capacitor C2) is 180° out of phase with the output voltage (across the capacitor C1), as the centre of the two capacitors is grounded. A phase shift of 180° is produced by the feedback network and a further phase shift of 180° between the output and input voltage is produced by the CE transistor. Hence, the total phase shift is 360° or 0°, which is essential for sustained oscillations, as per, the Barkhausen criterion. So we get continuous undamped oscillations.

Procedure:-The circuit is connected as shown in figure.



Connect the CRO across the output terminals of the oscillator. Switch on the power supply to both the oscillator and CRO. Select proper values of L, C1 and C2 in the oscillator circuit and get the sine wave form on the screen of CRO. The voltage (deflection) sensitivity band switch (Y-plates) and time base band switch (X-plates) are adjusted such that a steady and complete picture of one or two sine waveform is obtained on the screen. The horizontal length (l) between two successive peaks is noted. When this horizontal length (l), is multiplied by the time base (m) i.e. sec/div , we get the time-period (T = l x m).The reciprocal of the time-period(1/T) gives the frequency(f). This can be verified with the frequency, calculated theoretically by using the above formula. The experiment is repeated by changing L or C1 or C2 or all. The readings are noted in the table given.

Precautions:

1) Check the continuity of the connecting terminals before going to connect the circuit.
2) Identify the emitter, base and collector of the transistor properly before connecting it in the circuit.
3) The horizontal length between two successive peaks should accurately be measured.

RESULT: *Thus obtained the required values and ploted the graph.*

8. INVERTING AMPLIFIER

AIM:

To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

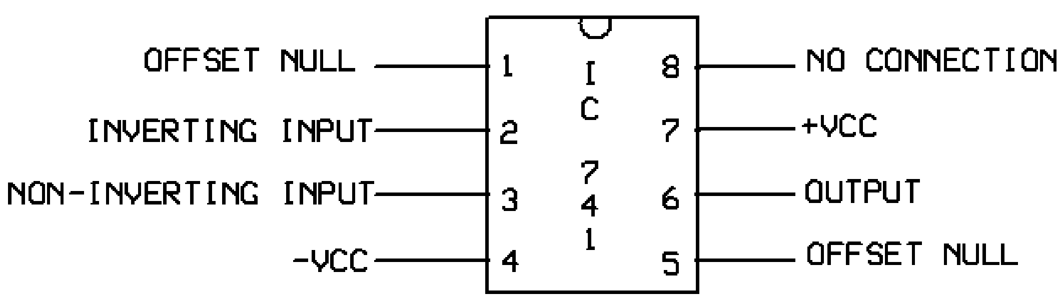
The input signal V_i is applied to the inverting input terminal through R_1 and the non-inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the R_f - R_1 network, where R_f is the feedback resistor. The output voltage is given as, $V_o = -A_{CL} V_i$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

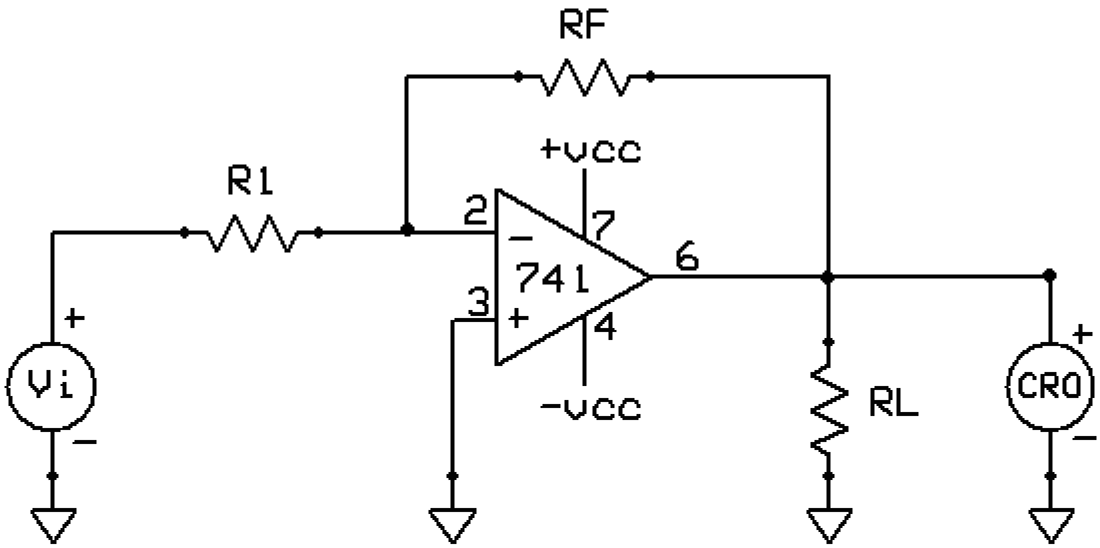
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



DESIGN:

We know for an inverting Amplifier $A_{CL} = R_F / R_1$

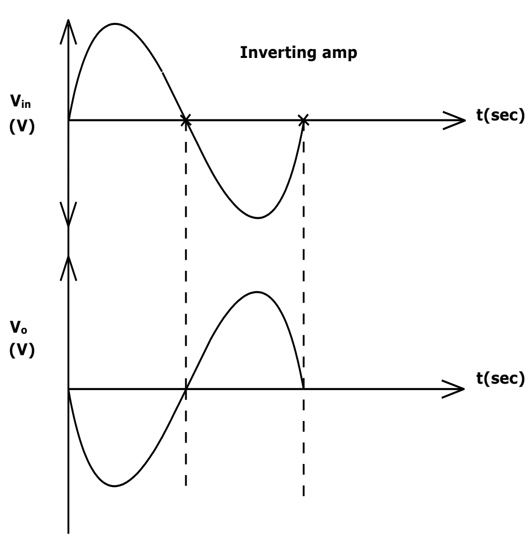
Assume R_1 (approx. 10 KΩ) and find R_f

Hence $V_o = - A_{CL} V_i$

OBSERVATIONS:

S.No	Parameters	Input	Output	
			Practical	Theoretical
1.	Amplitude(No. of div x Volts per div)			
2.	Time period(No. of div x Time per div)			

MODEL GRAPH:



RESULT:

9. NON - INVERTING AMPLIFIER

AIM: To design a Non-Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

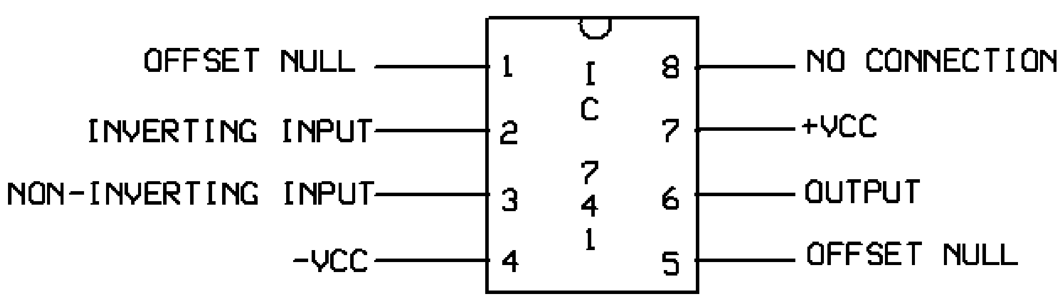
THEORY:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as, $V_o = A_{CL} V_i$, Here the output voltage is in phase with the input signal.

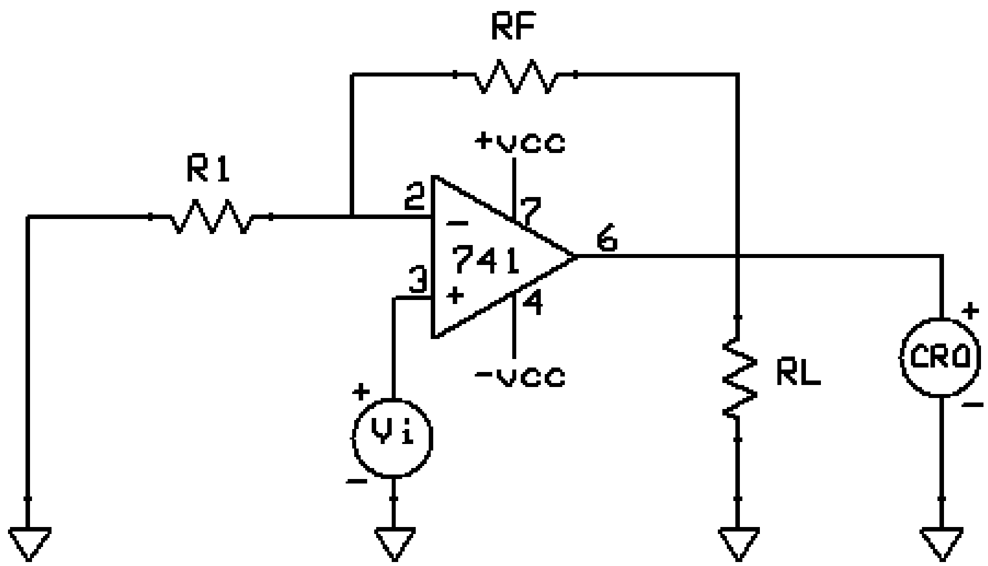
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF NON INVERITNG AMPLIFIER:



DESIGN:

We know for a Non-inverting Amplifier $A_{CL} = 1 + (R_F / R_1)$

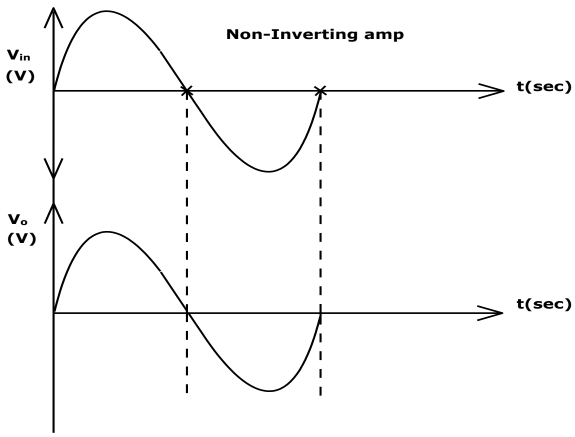
Assume R_1 (approx. 10 KΩ) and find R_f

Hence $V_o = A_{CL} V_i$

OBSERVATIONS:

S.No	Parameters	Input	Output	
			Practical	Theoretical
1.	Amplitude (No. of div x Volts per div)			
2.	Time period (No. of div x Time per div)			

MODEL GRAPH:



RESULT:

10. DIFFERENTIATOR

AIM: To design a Differentiator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

THEORY:

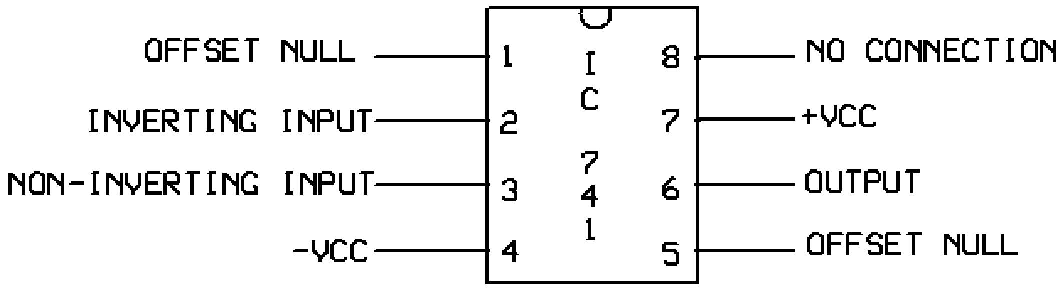
The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1. The expression for the output voltage is given as, $V_o = - R_f C_1 (dV_i /dt)$ Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. A resistor $R_{comp} = R_f$ is normally connected to the non-inverting input terminal of the op-amp to compensate for the input bias current.

A workable differentiator can be designed by implementing the following steps:

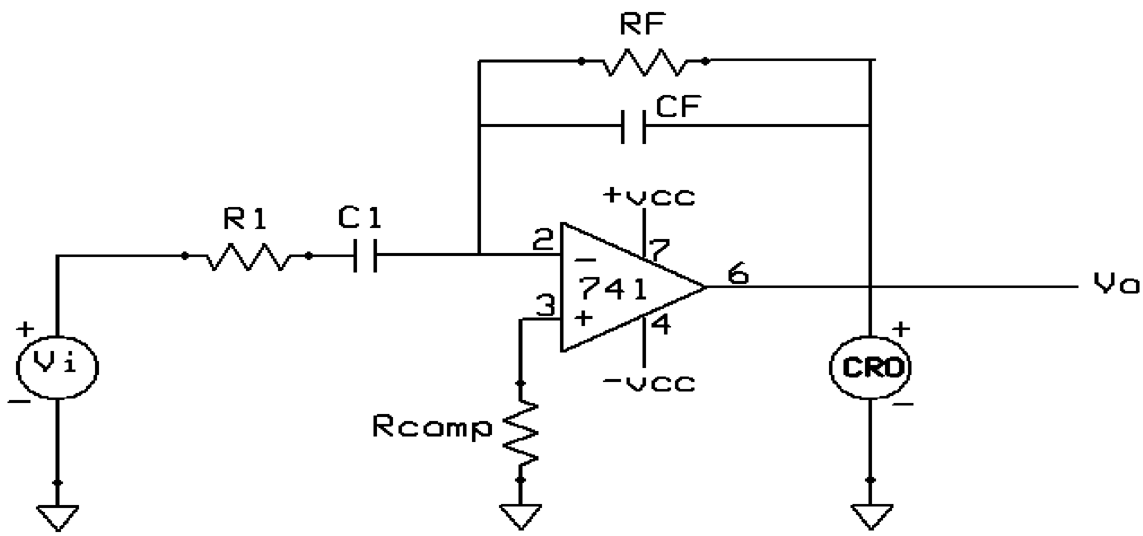
1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of $C_1 < 1$ µF, calculate the value of R_f.
2. Choose $f_b = 20 f_a$ and calculate the values of R_1 and C_f so that $R_1C_1 = R_f C_f$.

The differentiator is most commonly used in waveshaping circuits to detect high frequency components in an input signal and also as a rate–of–change detector in FM modulators.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF DIFFERENTIATOR:



DESIGN :

To design a differentiator circuit to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1 V peak at 1000Hz is applied to the differentiator , draw its output waveform.

Given $f_a = 1$ KHz

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_f C_1)$

Let us assume $C_1 = 0.1$ µF ; then

R_f = __________

Since $f_b = 20 f_a$, $f_b = 20$ KHz

We know that the gain limiting frequency $f_b = 1 / (2\pi R_1 C_1)$

Hence R_1 = __________

Also since $R_1C_1 = R_f C_f$; Cf = __________

Given $V_p = 1$ V and f = 1000 Hz, the input voltage is $V_i = V_p \sin \omega t$

We know $\omega = 2\pi f$

Hence $V_o = - R_f C_1 (dV_i /dt)$

$= - 0.94 \cos \omega t$

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No		Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

RESULT:

11. INTEGRATOR

AIM:

To design an Integrator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

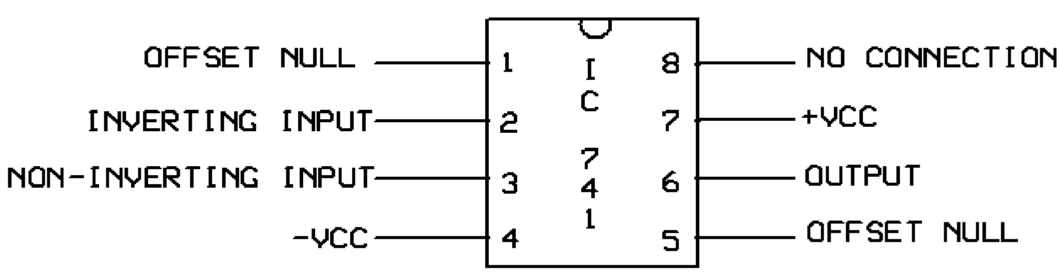
S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

THEORY:

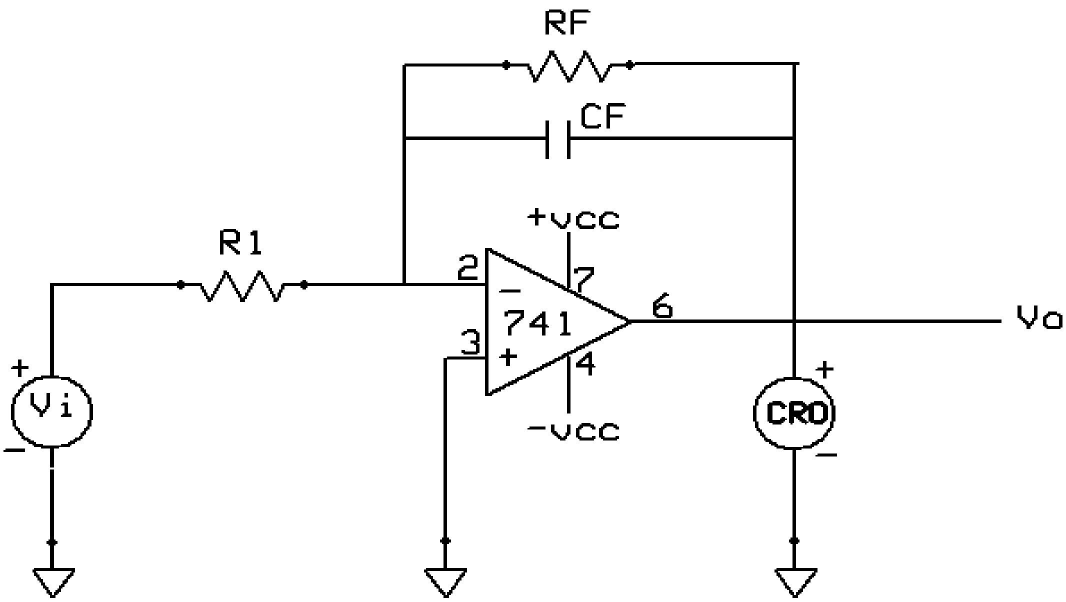
A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The expression for the output voltage is given as, $V_o = - (1/R_f C_1) \int V_i\, dt$ Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$.

That is, $T \geq R_f C_f$ The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INTEGRATOR:



DESIGN:

To obtain the output of an Integrator circuit with component values $R_1C_f = 0.1ms$, $R_f = 10\ R_1$ and $C_f = 0.01\ \mu F$ and also if 1 V peak square wave at 1000Hz is applied as input.

We know the frequency at which the gain is 0 dB, $f_b = 1 / (2\pi\ R_1\ C_f)$

Therefore f_b = _____

Since $f_b = 10\ f_a$, and also the gain limiting frequency $f_a = 1 / (2\pi\ R_f\ C_f)$

We get , R_1 = _______ and hence R_f = __________

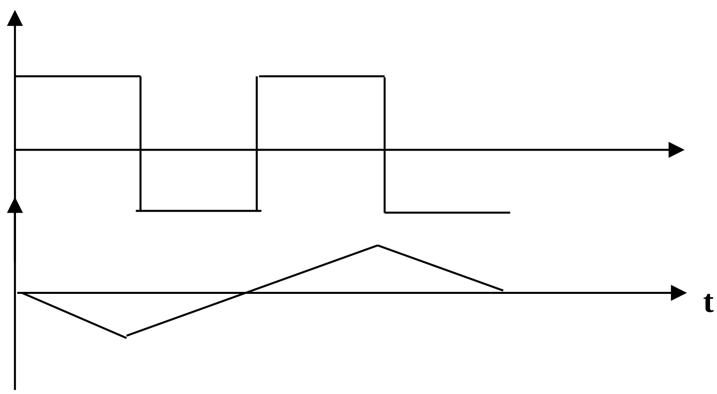
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No		Input	Output
1.	Amplitude(No. of div x Volts per div)		
2.	Time period(No. of div x Time per div)		

MODEL GRAPH: **INTEGRATOR**



RESULT:

This lab manual has been updated by

Dr. K. K. Shukla
(kaustubh.shukla@gnindia.dronacharya.info)

Crosschecked By
HOD ECE

Verified By
Director, DGI Greater Noida

Please spare some time to provide your valuable feedback.